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In Stock! Advanced I/O Receiver Module IC600Y IC600YB

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DESCRIPTION OF OPERATION

The Advanced I/O Receiver module (IC600BF830B) is designed to be placed into the left most slot of an I/O rack and has the ability to perform all the functions of the Standard I/O Receiver module (IC600BF800B) plus many additional fault diagnostic functions.

NOTE

The default switch settings on this module have all the advance features disabled, thus, permitting the module to respond as if it were a Standard I/O Receiver module (IC600BF800B).

To access the diagnostic information of the Advanced I/O Receiver module, the user must assign the module an Input and Output address location. Two 7-segment dip switches are provided on the lower right hand corner of the module for this purpose. One set of dip switches is used to select an Input address, while the other set is used to select an Output address. Unlike I/O modules the addresses DO NOT have to be the same, although identical addresses can be selected. The 7-segment switches are set in the same pattern as that used for standard I/O addressing. It is important to note that the I/O address accessibility is not enabled until SW3 on a third "Option Select" dip switch is set to the enabled position. The default address setting is I/O 993.

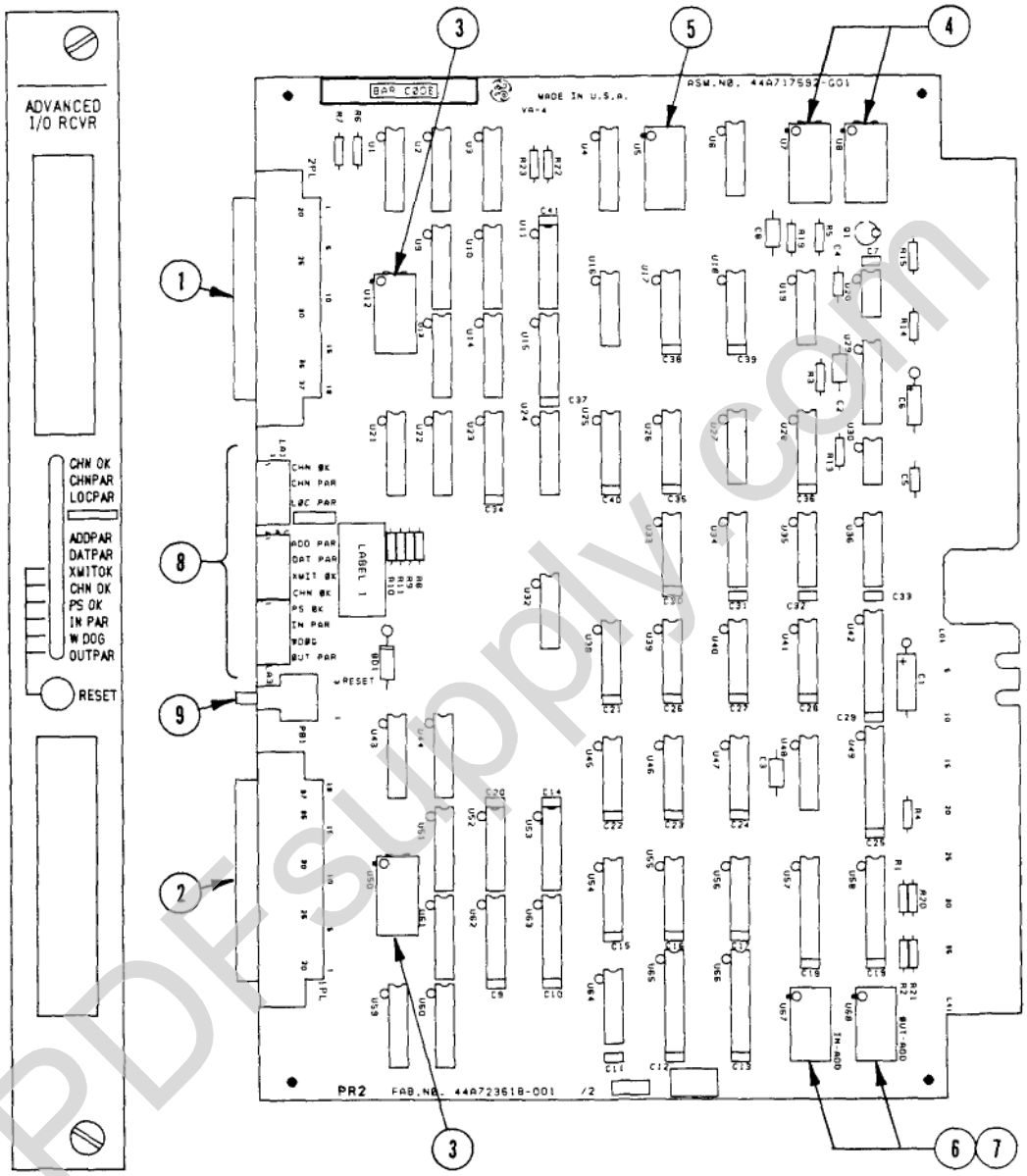
When the Advanced I/O Receiver module is placed in an I/O rack there are two 37-pin connectors available through the faceplate. The top connector receives an I/O cable that is connected to an upstream I/O rack or directly to the CPU. If coming from another upstream I/O rack, it may be connected to a Standard or Advanced I/O Receiver module, or to a Local I/O Transmitter module. The bottom connector can be left unconnected, connected to a Standard or Advanced I/O Receiver module, or be connected to a Workmaster Programmer or Program Development Terminal. Any of the above modules can be connected and intermixed to meet the requirements of a given application. On both the Standard and Advanced I/O Receivers, the top and bottom connectors are internally connected together, thus, data signals can pass through them even though the I/O rack may be nonfunctional. In the Advanced module, data can also pass through even if the power supply is turned off.

Located on the Advanced I/O Receiver module are two identical dip resistor pacs whose socket locations determines if the module is used in an intermediate I/O rack or used in the last rack of a given I/O chain. The module is configured for use in an intermediate rack when the dip resistor pacs are located in sockets U7 and U8 (default positions). When configured as the last rack in an I/O chain, the resistor pacs must be located in sockets U 12 and U50. The resistor pacs are identical and thus can be interchanged.

Refer to Table 1 and Figure 1 for module specification and user component layout.

Table 1
MODULE SPECIFICATIONS

Dimensions: Circuit Board: 8.15 x 11.0x 1.20 (inches) 208 x 280 x 31 (mm) Faceplate: 12.46 x 1.175 (inches) 317 x 30 (mm) Power Requirements: 5VDC, 680 mA typical, 1.2A maximum, supplied by I/O rack power supply	Operating Temperature: 0 - 60°C (outside of rack) Storage Temperature: - 2 C - +80°C Humidity: 5% - 95% non-condensing



1 D-type 37-pin connector to upstream modules
2 D-type 37-pin connector to downstream modules
3 Resistor pac locations for last I/O rack in chain.
4 Resistor pac locations for intermediate I/O rack in chain.
5 Dip switch for selection of module options.
6 Dip switch for selection of Input address.
7 Dip switch for selection of Output address.
8 Location of 12 LED diagnostic indicators.
9 Location of external Reset pushbutton.

Figure 1
LOCATION OF USER ITEMS

Twelve LED diagnostic indicators, visible through the faceplate, are mounted on the Advanced I/O Receiver module. These LED's are used to indicate status and the results of diagnostic routines executed by the module. The last six indicators are latched-in (or turned off) when a fault is sensed as some faults may be transitory or intermittent. These latched-in fault indications can be reset (if the fault is cleared) by depressing the RESET pushbutton that is accessibIe through the faceplate, or by CPU logic sending a latch reset signal through the I/O chain, This signal is read by the module via the I/O addresses that have been previously set and enabled. Cycling the power of the rack that contains the module will also reset the LED indicators. Note that the power supply OK LED indicator will be latched off when this is done. The following table describes the function of each diagnostic indicator.

Table 2
LED INDICATORS

CHN OK	– CHAIN OKAY, ON if power is okay in all downstream racks, and if cable continuity is okay to all downstream racks; OFF if one of the above conditions is not met.
CHNPAR	– CHAIN PARITY, ON if Output Parity is okay on rack backplane; OFF if Output Parity Error is sensed from a Local Transmitter or Remote I/O Driver in this rack.
LOCPAR	– LOCAL PARITY, ON if Output Parity is okay in this rack; OFF if this module has detected an Output Parity Error entering from an upstream rack.
BLANK	– The state of this LED is controlled by CPU logic and transmitted to the module via its I/O address. The default state of this LED is ON.
ADDPAR	– ADDRESS PARITY, ON if no error is detected in the I/O address transmitted from the CPU through the l/O chain; OFF if a Parity Error is detected in the T/O address transmitted from the CPU. Successful retransmission of the address will clear the Parity Error.
DATPAR	– DATA PARITY, ON if no error is detected in the I/O data transmitted from the CPU through the I/O chain; OFF if a Parity Error is detected in the I/O data transmitted from the CPU. Successful retransmission of data will clear Parity Error.
XMITOK	– TRANSMIT OKAY, ON if power is okay and cable continuity is okay to all downstream racks connected to a Local Transmitter or Remote I/O Driver module that is located in this rack; latched OFF if the above conditions are not met in one or more of the connected racks.
CH OK	– CHAIN OKAY, ON if power and cable continuity is okay to all downstream racks directly connected to this Advanced I/O Receiver; latched OFF if the above conditions are not met in one or more of the connected racks.
PS OK	– POWER SUPPLY OKAY, ON if power supply in this rack is within tolerance; latched OFF if power supply should fall out of tolerance. LED will be latched off when power is applied to power supply.
IN PAR	– INPUT PARITY, the source of Input Parity Error is determined by the settings of SW6 and SW7 of the diagnostic dip switch; the LED is ON if no Input Parity Error is sensed; latched OFF if an Input Parity Error is sensed from either a Local I/O Transmitter or Remote I/O Driver module mounted in this rack, or from any downstream I/O rack that may be connected directly to the Advanced I/O Receiver module in this rack.
W DOG	– WATCH DOG TIMER, ON when communications to the CPU is okay; iatched OFF if the module has not communicated to the CPU within the last one second.
OUTPAR	– OUTPUT PARITY, ON if no Parity Error is detected in either the I/O address or I/O data transmitted from the CPU; latched OFF if a Parity Error is detected. This is a latch for ADDPAR and DATPAR indicators previously discussed.

Before discussing the selectable options available when using the Advanced I/O Receiver module, an understanding of Series Six CPU I/O diagnostics is required. Three I/O fault types are recognized by the CPU. They are:

Input Parity fault
Output Parity fault
I/O Chain fault,

The following discussion explains CPU and I/O fault response when using the Standard I/O Receiver module (IC600BF800B).

Input Parity can only be sensed by the CPU, and, when detected as an error, the CPU will issue a RESET command, and then, goto a STOP condition. The RESET command is sent to all I/O racks and will turn off all outputs except for those on a module that can be selected to Hold Last State, The input parity setting is first set in the I/O Receiver module of the rack which contains that I/O address. If the CPU calculates a different parity, it will automatically perform a single retry. If this retry also returns with a parity error, the CPU will set the Input Parity Fault bit, store the input address, issue a RESET command to the I/O bus and enter a STOP state.

Output Parity is sensed by each I/O Receiver module, even if its I/O rack wasn't set to the output address that the parity error was detected in. The output parity setting is first set in the CPU and sent to the I/O chain with every output address and data byte. If an I/O Receiver module detects an Output Parity error (CHNPAR LED), a signal will be returned to the CPU and a single retry will be attempted. If the error remains, the CPU will set the Output Parity Fault Bit, stores the output address, and issues a RESET command to the I/O bus forcing all outputs off, unless they are connected to a module which can select Hold Last State. After a RESET signal is sent, the CPU will goto a STOP condition. A Parallel Transmitter or a Remote Driver module can also detect Output Parity errors (LOCPAR LED) and issue the Parity Error signal to the CPU.

I/O Chain faults (CHN OK LED) can be sensed in any I/O Receiver module. The module is designed to detect downstream power supply faults, and faults in the I/O cable continuity, both of which will cause the I/O Chain Fault signal to be returned to the CPU. If this signal is received by the CPU, a RESET command will be issued to the I/O bus forcing all outputs off, unless they are connected to a module which can select Hold Last State. After the RESET signal is sent, the CPU will goto to a STOP condition.

Keeping the above facts in mind, the following will explain the function of each of the eight selections available on the Option Select dip switch located at the top center of the Advanced I/O Receiver module. The module is shipped with all eight switches in the closed or disabled position, allowing the module to perform only as a Standard I/O Receiver module. A table guide and explanation of the Option Select switches follows.

SWITCH 1: Disable downstream I/O Chain Fault.

SWITCH 2: Disable I/O Chain Fault from backplane.

SWITCH 3: Enable Diagnostics

SWITCH 4: Disable return of Output Parity.

SWITCH 5: Disable Watchdog Timer RESET to backplane.

SWITCH 6: Enable local parity error to turn on 'IN PAR' LED.

SWITCH 7: Enable I/O Chain Parity to turn on 'IN PAR' LED.

SWITCH 8: Not used.

SWITCH 1:

The Series Six I/O system has extensive error checking logic to verify that each rack has a functional power supply, and that each I/O cable is connected. The I/O Receiver modules are designed to check for downstream power supply and cable failures of racks connected in a daisy chain from the lower connector of the module and, issue an I/O Chain Fault signal to the CPU if a problem is detected. A failure of this type can mean a loss of a major portion of the control system, and thus, the CPU is normally setup to issue a RESET command and goto a STOP condition when an I/O Chain Fault signal is received. Switch 1 selects what the module does with this signal when it is received at the bottom cable connector. When **CLOSED,** the signal is passed through on towards the CPU and, unless intercepted by another Advanced I/O Receiver module upstream, will cause the CPU to issue a RESET command. Both CHN OK LED's will be turned off or latched off. If set in the **OPEN** position, the signal will be blocked, thus, allowing the CPU to continue to scan. With this switch setting, the first CHN OK LED will remain on, and the second CHN OK LED will be latched off and Bit 2 in the Input byte is set to a ' I'.

SWITCH 2:

The Series Six I/O system can also detect power supply and cable faults in I/O racks that are connected to the system via Local Transmitter or Remote I/O Driver modules. These downstream faults, if not inhibited by an Advanced I/O Receiver, are passed through the above modules and via the rack backplane to the Receiver module located in that rack. From here, the signal is passed upstream until it reaches the CPU, or is blocked by another Advanced Receiver module. This I/O Chain Fault signal, when received by the CPU will react as described above. Switch 2 selects what the module does with this signal when received from either a Local Transmitter or Remote I/O Driver module. When **CLOSED,** the signal is passed through the module to the next I/O rack or to the CPU. If a error is sensed, the CHN OK LED will be turned off, and the XMITOK LED will be latched off. If set in the OPEN position, the signal will be blocked, thus allowing the CPU to continue to scan. Whenever this fault is sensed, the CHN OK LED will remain **on, and** the XMITOK LED will be latched off and Bit 1 of the Input **byte is** set to a '1'.

SWITCH 3:

This switch provides overall control of ALL diagnostics provided by the Advanced I/O Receiver module. If **CLOSED,** the module will perform as a Standard I/O Receiver module (IC600BF800B), and, no additional diagnostics will occur. When set to the **OPEN** position, the diagnostic features selected via the other switches will be enabled, and, the I/O addresses selected on the remaining two 7-segment dip switches will be activated. In either switch setting, the LED indicators will all be active.

SWITCH 4:

All I/O data transfers are protected by a parity bit that is attached to the input or output data byte, and in the case of outputs, parity is also checked on the address byte. Parity is set at the sending end and verified by each module that it passes through. Input data parity returning to the CPU is checked at every Advanced I/O Receiver it passes through. If a parity fault is sensed, that module will latch off the IN PAR LED and set an internal bit that may be transferred to the CPU signaling the location(s) that sensed the error. An Input Parity error received by the CPU, after a second retry, will cause a RESET command to be sent to the I/O Chain followed by the CPU going to a STOP condition. Only with Level 105 or higher CPU software can this be prevented. Output Parity is checked at every I/O Receiver module the data passes through. Switch 4 determines what the module will do if it senses an Output Parity Error. In the CLOSED position, the module will sense a parity error and send the Output Parity Error signal up the chain to the CPU. The OUTPARLED will be latched off and either the ADDPAR or DATPAR LED will turn off. This Output Error signal will cause the CPU, after a second retry, to issue a RESET command and then goto a STOP condition. In the **OPEN** position, the Output Parity Error signal will be blocked from going upstream to the CPU only if the source of the error is from an upstream connection. Both the CHNPAR and LOCPAR LED's will remain on, while the ADDPARor DATPAR, and OUTPARLED's will turn off. Bit 6 of the Input byte is set to a '1'.

SWITCH 5:

The Advanced I/O Receiver module is provided with a built-in Watchdog Timer, similar to the one built into all CPU's The timer is reset whenever the I/O channel is accessed. If this Watchdog Timer should time out, 1 second +/-IO%, it will issue an internal RESET command to this rack (if not blocked) and to any rack connected via a Local Transmitter or Remote I/O Driver module. Upstream and downstream racks connected directly to the Advanced I/O Receiver module will not be effected. In effect, the rack has failed to communicate to the CPU for at least 1 second. CPU's that have their power shut off or an internal fault, or if an I/O cable should fail would cause the Watchdog Timer to time out. A CPU that had its keyswitch turned to the STOP position would not cause the timer to time out. Thus, in the unlikely event that the CPU should stop scanning, and the rack Output Enable line is set high, this timer would prevent outputs from being uncontrollably left on for long periods of time. Output devices that are set to Hold Last State, and have user power connected, will not be reset by the Watchdog Timer. The function of Switch 5 is to determine what to do with this signal if the timer should time out. In the CLOSED position, this signal will be blocked and will have no effect on the outputs. In the OPEN position, the RESET signal from the Watchdog Timer will be issued to the backplane causing its outputs and those connected via Local Transmitters or Remote I/O Drivers to be forced off. The W DOG LED will be latched off if this Watchdog Timer should ever time out. Bit 5 of the Input byte is set to 'I'.

SWITCH 6 and 7:

The IN PAR LED is controlled from two different internal signals. The first signal, controlled by Switch 6, comes from the rack backplane and contains an Input Parity Error that was received by a Local Transmitter or Remote I/O Driver. The second signal, controlled from Switch 7, comes from the bottom connector of the module and senses Input Parity Errors from a downstream rack. The function of switches 6 and 7 is to determine what signal(s) drive the IN PAR LED. In the CLOSED position, the signal is allowed to latch the LED off. The default setup allows both signals to drive the LED. If the OPEN position is set, the signal will be blocked, If both switches are open, no signal will be applied and the LED will remain ON with no function. Bit 4 of the Input byte will be set to a '1' if an Input Parity Error is detected.

SWITCH 8:

This switch has no function, but *must* be closed.

I/O ADDRESS FUNCTIONS

If the Advanced I/O Receiver module is set to use any or all of its advanced diagnostic functions (SW 3 of the Option Select switches set to OPEN), it will be required to use one or both of the Input and Output addresses selected by the individual dip switches on the module. Any valid I/O address can be selected. Refer to GEK-25361, Installation and Maintenance Manual, for details. The state of the output data (0 or 1) is controlled by the CPU relay logic entered by the user. The state of the input data bits (0 or 1) is controlled by the individual Advanced I/O Receiver modules. Tables of Input and Output bit assignments and a description of their use follows. Each address byte contains 8 bits of data, with bit 1 being the least significant bit.

Table 4
INPUT ADDRESS BYTE

BIT 1:	Set if Chain I/O Fault is sensed from backplane.
BIT 2:	Set if Chain I/O Fault is sensed from downstream rack connected to the bottom connector of the module.
BIT 3:	Set if rack power supply is out of tolerance or if power is turned on or restored to the rack.
BIT 4:	Set if Input Parity is sensed from any location.
BIT 5:	Set if Watchdog Timer times out.
BIT 6:	Set if Output Parity is detected.
BIT 7:	Set if resister pacs are set for intermediate rack.
BIT 8:	Set at all times to indicate an Advanced Receiver.

INPUT BYTE, BIT I: This bit is set to a '1' if an I/O Chain Fault is sensed on the backplane of the rack. The fault signal will come from either a Local Transmitter or a Remote I/O Driver module. Refer to Switch 2 and to LED's CHN OK and XMITOK. This bit will remain set to '1' as long as the XMITOK LED is latched off. The module will set this bit to '0' if a latch reset signal is received, if the Reset pushbutton is depressed, or if rack power is cycled.

INPUT BYTE, BIT 2: This bit is set to a ' 1' if an I/O Chain Fault is sensed coming from a downstream rack connected to the bottom connector of the module. Refer to Switch I and to LED's CHN OK and CHN OK. This bit will remain set to a 'I' as long as the CHN OK LED is latched off, The module will reset this bit to a '0' if a latch reset signal is received, if the Reset pushbutton is depressed, or if rack power is cycled.

INPUT BYTE, BIT 3: This bit is set to a '1' if the rack power supply is out of tolerance or if power has been cycled to the rack. Refer to PS OK LED. This bit will remain set as Iong as the PS OK LED is latched off. The module will set this bit to a '0' if 3 latch reset signal is received, if the Reset Pushbutton is depressed, or if rack power is cycled.

INPUT BYTE, BIT 4: This bit is set to a '1' if an Input Parity Error is sensed from either a Local Transmitter, a Remote I/O Driver, or from a downstream rack connected to the module. Refer to Switches 6 and 7 and LED IN PAR. This bit will remain set as long as the IN PAR LED is latched off. The module will set this bit to a '0' if a latch reset signal is received, if the Reset Pushbutton is depressed, or if rack power is cycled.

INPUT BYTE, BIT 5: This bit is set to a '1' if the on board one second Watchdog Timer has timed out. Refer to Switch 5 and LED W DOG. This bit will remain set as long as the W DOG LED is latched off. The module will set this bit to a '0' if a latch reset signal is received, if the Reset Pushbutton is depressed, or if rack power is cycled.

INPUT BYTE, BIT 6: This bit is set to a '1' if an Output Parity Error is detected on the module in a signal coming in from an upstream rack. Refer to Switch 4 and LEDs CHNPAR, LOCPAR, and OUTPAR. Output Parity errors from downstream racks will not set this bit. This bit will remain set as long as the OUTPAR LED is latched off. The module will set this bit to a '0' if a latch reset signal is received, if the Reset Pushbutton is depressed, or if rack power is cycled.

INPUT BYTE, BIT 7: This bit is set to a '1' only if the two identical dip resistor pacs are located in sockets U7 and US for use as an intermediate I/O rack. This bit is set to a '0' if the above condition is not true.

NOTE: If the dip pacs are not installed, or are improperly installed, the bit will be set to '0'.

INPUT BTYE, BIT 8: This bit is set to a '1' at all times and cannot be changed or reset. This bit is used to indicate to the CPU that an Advanced I/O Receiver module is

Table 5
OUTPUT ADDRESS BYTE

BIT 1: If set, the CPU logic RESET command is sent.
BIT 2: If set, the LED latches will be cleared.
BIT 3: If set, the User LED will come on.
BIT 4: If set, the module will write data to its Input add.
BIT 5: If set, the module will block the CPU RESET command.
BIT 6: If set, the module will not send local input data.
BIT 7: If set, disable I/O Chain Fault from connector.
BIT 8: If set, disable I/O Chain Fault from backplane.

OUTPUT *BYTE,* BIT 1: If set to a '0', no action is taken by the module. If set to a 'I', the module will react as if the CPU has sent a RESET command and will turn off all outputs in its rack and all outputs connected via a Local Transmitter or Remote I/O Driver. Output modules set to Hold Last State will not be effected. This RESET state will be held until this bit is set to a '0' value.

OUTPUT BYTE, BIT 2: If set to a '0', no action is taken by the module. If set to a 'I', the module will reset all LED latches, thusly, turning on any of the six LED's that may have been latched off, and removing from the Input byte any associated data. A leading edge trigger is used and latches will reset if the fault is not cleared. For maximum efficiency, it is desirable to have the input address byte less than or equal to the output address byte. Refer to Output Bit 4 where the opposite is true.

OUTPUT BYTE, BIT 3: This bit controls the state of the User LED. If set to a '0' the LED will be on. If set to a 'l', the LED will turn off. The User LED is controlled by the user's relay logic program and may be used to indicate which rack requires servicing based upon analysis of diagnostic data returned, or may merely turn on or flash to obtain an operator's attention. The User LED is the 4th LED down from the top.

OUTPUT BYTE, BIT 4; If this bit is set to 'O', the module will NOT send its Input data bits when the selected lnput address is polled. This bit MUST be set to a '1' for this data to be returned to the CPU. This function *is* provided so that several Advanced I/O Receiver modules can be multiplexed to the CPU using only one Input address byte. In this example, each module must have a different Output address so the CPU can select which module it wishes to receive data from. This function will help conserve valuable input addresses. When using this function to multiplex data, the output addresses must be lower than or equal to the input address.

OUTPUT BYTE, BIT 5 This bit is used to control the CPU RESET command which is sent whenever the CPU detects an internal fault or an external I/O Chain Fault or Parity Error, or if power is removed from the CPU. If this bit is set to a '0', the module will respond to this RESET signal and turn off all outputs in its rack and those connected via a Local Transmitter or Remote I/O Driver module. The RESET signal will pass through to downstream racks. Modules with Hold Last State set will not be effected. Also, a downstream Advanced I/O Receiver module may block transfer of this signal into its rack. If this bit is set to a 'l', the module will ignore the CPU RESET command, and all outputs will remain as set. The RESET signal is still passed through the bottom connector to downstream racks. If this output bit is set, and the CPU shuts down, the outputs will remain set for one second until the module's local Watchdog Timer times out.

Note: Switch 5 can disable the Watchdog Timer reset signal, and thus, ALL outputs will remain in a Hold Last State condition.

OUTPUT BYTE, BIT 6: Ii this bit is set to '0', the module will take no action. If set to a 'I', ALL Input data from Input modules plugged into this rack will be prevented from going to the CPU Input Table. Using this bit, inputs from multiple racks can be multiplexed into identical addresses. This feature also allows the tracking down of modules that are mistakenly set to the same input address.

OUTPUT BYTE, BIT 7: If this bit is set to '0', the module will take no action. If set to a 'I', it will have the same effect as Switch 1 and prevent an I/O Chain Fault, coming from the rack backplane, to be transmitted upstream to the CPU.

OUTPUT BYTE, BIT 8 If this bit is set to '0', the module will take no action. If set to a 'l', it will have the same effect as Switch 2 and prevent an I/O Chain Fault, coming from a downstream rack connected to the bottom connector of the module, to be transmitted upstream to the CPU.

CPU SOFTWARE LEVEL 105 OR HIGHER

In addition to the flexibility provided by the Advanced I/O Receiver module, changes in the CPU executive program must also be made if full diagnostic advantage is to be taken. In CPU software levels up to Level 104, the CPU is instructed to goto a STOP state whenever it reads two consecutive input or output parity errors on the same address or data byte. With the diagnostic functions made available with this module, this mandatory STOP feature may not be required or desired. A user diagnostic program can pinpoint the source of the problem, isolate it, force it to a safe or known condition, and thusly, allow the CPU to remain in RUN and execute control over the remaining I/O structure. Level 105 software (or above) will allow the user to have this level of control over the Series Six CPU.

Level 105 software takes advantage of the STATUS function and uses it in the following manner.

```
                Rnnnn
——] [———[STATUS]
                HHHH
```

When continuity is made to the STATUS function, the bits of Rnnnn take on the following meaning.

BIT 16: 0 - Level 105 enhancements are disabled.
1 - Level 105 enhancements are enabled.

BIT 15: 0 - Noaction.
1 - Set I/O Parity retries to the number set in Bits l-8.

BIT 14: 0 - No action.
1 - DO NOT stop CPU upon detection of I/O Parity fault even though all retries have failed. Input table will remain unchanged.

BITS 9-13: No function defined.

BITS l-8: Contains retry attempts, O-255. If 0, a single retry will be attempted.

When continuity is not made to the STATUS function, the bits of Rnnnn take on the following meaning.

BIT 16: 0 - Level 105 software not enabled.
l– Level 105 software is enabled.

BIT15: O- No Parity Error has occurred.
l– An I/O Parity Error occurred since the last time STATUS was read. It will be set even if the retry was successful.

BIT 14: 0 - No Parity Error has occurred.
l– An I/O Parity Error occurred since the last time STATUS was read and the prescribed number of retries were unsuccessful.

BITS 9-13: No function defined

BITS l-8: Contains the address of the last Parity Error or the last Memory Parity Error.

If Bit 16 is set to a 'l', and continuity is made to the STATUS function, the lower 8 bits will set the number of retries for a parity error. If continuity is not made, the lower 8 bits will display the number of retries. If Bit 16 is set to a '0', and continuity is made to the STATUS function, the DPU and CCM windows can be controlled. If continuity is not made, the lower 8 bits will display the status of the above window selection.

ORDERING [NFORMATION

CIRCUIT BOARD AND FACEPLATE	JC600BF830B
CIRCUIT BOARD ONLY	IC600YB830B
FACEPLATE ONLY	IC600FP830B

For specific ordering information and application assistance, contact your local GE Fanuc sales office.

GE Fanuc Automation North America, Inc., Charlottesville, Virginia

MARCH, 1985