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In Stock! High Speed Counter Module IC600B IC600BF

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TABLE 1, FEATURES AND BENEFITS

FEATURES	BENEFITS
Accepts many types of counting input Quadrature encoder Digital tachometer Transistor/photo switch Mechanical contacts	Provides direct and isolated inputs for multiple types of field devices
Counting rate to 50KHz X1, X2, X4 count input for quadrature input to 200KHz Maximum count: -8,388,608 to + 8,388,607	Provide high speed pulse input over wide count range, no need to cascade counters
Four external outputs Individual preset comparisons can be <, or \geq to accumulated count Individual enable/latch functions .500 micro-second response time Sink 250ma, TTL to 30VDC	Control multiple field devices, for fast, high speed application
Eight internal presets for CPU use Individual preset comparisons can be <, or \geq to accumulated count	Functions as programmable limit switch whose bits can be read by the CPU and used to control logic based on accumulated count.
Internal/External Signals for Count enable Count direction Count reset Marker Home position	Added dimensions for flexible, real world applications
Calculate the number of counts occurring during a user-defined time period.	Returns counts/timebase (velocity) value for use in digital speed regulation programs
Continued operation of counter if CPU is placed off-line or fails	Maintain accurate position count and control of connected loads
Built-in diagnostics, indicators and CPU status information	Detects system faults and alerts CPU logic and operator

TABLE 2. SPECIFICATIONS

<p>Dimensions:</p> <p>Circuit Board 8.15 x 11.0 x 1.20 (inches) 208 x 280 x 31 (mm)15.0V</p> <p>Faceplate 12.46 x 1.175 (inches)0.2V 317 x 30 (mm)</p> <p>Power requirements 5 VDC, 1.1A maximum Supplied by I/O rack power supply Units of Load = 19 User Supplied</p> <table border="0"> <tr> <td>TTL</td> <td>1 0-30v</td> </tr> <tr> <td>Voltage</td> <td>5V + 0.20 VDC 10-30V ± .5 VDC</td> </tr> <tr> <td>Ripple</td> <td>100mv Iv</td> </tr> <tr> <td>Current</td> <td>400ma 400ma</td> </tr> </table> <p>Timing Characteristics Input Pulse Rate: DC to 50KHz (square wave) Input Pulse Rate with filter selected: DC to 100Hz (square wave) Marker Pulse Width: 5 usec (minimum) Response time for outputs 1-4 to incoming pulses: 500 usec (typ)</p> <p>TTL Single Ended Sink Input Characteristics Maximum Input Voltage: 5.5V Minimum Turn-On Voltage: 2.0V Minimum Input Voltage: -1.5V Maximum Turn-Off Voltage: 0.8V Input Impedance: 1000 ohms (TYP) Minimum Low Level Input Current: -6.0ma (sinking)</p>	TTL	1 0-30v	Voltage	5V + 0.20 VDC 10-30V ± .5 VDC	Ripple	100mv Iv	Current	400ma 400ma	<p>5 Volt Differential Input Characteristics Inputs are RS422 compatible Maximum Input Voltage: ± 15.0V Common Mode Voltage Range: ± 7.0V Threshold Sensitivity: ± 0.2V Input Impedance: 115 ohms (TYP.) Minimum Input Current: ± 3.0ma</p> <ul style="list-style-type: none"> ● 10-30V single ended source input characteristics. <p>Maximum Input Voltage: 33V Minimum Turn-On Voltage: 9V Minimum Input Voltage: -20V Maximum Turn-off Voltage: 2V Input Impedance: 3800 ohms (TYP)</p> <ul style="list-style-type: none"> ● Output Characteristics Outputs are open collector with a common clamp diode (CLP) provided for optional connection to positive source. <p>Pull-up resistors provided for outputs. PU1 - 1100 ohm. PU2, PU3, outputs. PU4 = 4700 ohm</p> <p>Maximum Supply Voltage: 30 VDC</p> <p>Maximum On-State Voltage Drop: 0.4V for: I 50ma 0.70 for: 1250ma</p> <p>Maximum Output Current: 250ma continuous 500ma peak for 1 second</p> <ul style="list-style-type: none"> ● Operating Temperature: 0-60°C (at outside of rack) ● Storage Temperature: -20° to + 80°C ● Humidity: 5-95% (non-condensing) ● Altitude: Up to 10,000 feet above sea level
TTL	1 0-30v								
Voltage	5V + 0.20 VDC 10-30V ± .5 VDC								
Ripple	100mv Iv								
Current	400ma 400ma								

INSTALLATION

The High Speed Counter module can be installed in an I/O rack or in a Model 60 CPU rack. Before installing the module, the dual-in-line-package (DIP) switches immediately behind the card slot on the rack backplane should be set to reserve a group of 32 consecutive bits in the appropriate Input AND Output Status Tables of the CPU. For specific DIP switch settings, refer to Figure 1.

You should also set the circuit board jumpers and dip switch to configure the module for your particular application. Refer to Figure 2 for description of all user settings.

We recommend that you use the extraction/insertion tool furnished with your CPU to remove or install the circuit board. With the board in place in the rack, the edge connector on the faceplate should be slipped over the circuit board so that proper contact is made. You can then secure the faceplate to the rack using the thumbscrews at the top and bottom.

Refer to Figure 3 and 4 for typical user output connections to this module. Figure 7 shows the general internal design for the four output circuits, while Figures 5 and 6 contains the general internal design for the input circuits.

WARNING

Voltages from user field devices could be present on the faceplate terminals, even if the power supply in the I/O rack is off. Care should be taken when handling the faceplate of this module or any wires connected to it.

OUTPUT NUMBER	DIP SWITCH POSITION					OUTPUT NUMBER	DIP SWITCH POSITION					OUTPUT NUMBER	DIP SWITCH POSITION				
	7	6	5	4	3		7	6	5	4	3		7	6	5	4	3
1- 32						353-384	X	X	X			705-736	X	X	X		
33- 64				X		385-416	X	X				737-768	X	X	X	X	
65- 96			X			417-448	X	X	X			769-800	X	X			
97-128			X	X		449-480	X	X	X			801-832	X	X			X
129-160		X				481-512	X	X	X	X		833-864	X	X		X	
161-192		X	X			513-544	X					865-896	X	X		X	X
193-224		X	X			545-576	X			X		897-928	X	X	X		
225-256		X	X	X		577-608	X		X			929-960	X	X	X		X
257-288	X					609-640	X		X	X		961-992	X	X	X	X	
289-320	X			X		641-672	X	X			993-1024 } (NOT USED)	X	X	X	X	X	X
321-352	X	X			673-704	X	X	X									

= Switch in OPEN Position (Depressed to the Left)
Switches No. 1 and No. 2 should be in CLOSED Position

FIGURE 1. DIP SWITCH SETTINGS FOR I/O RACK

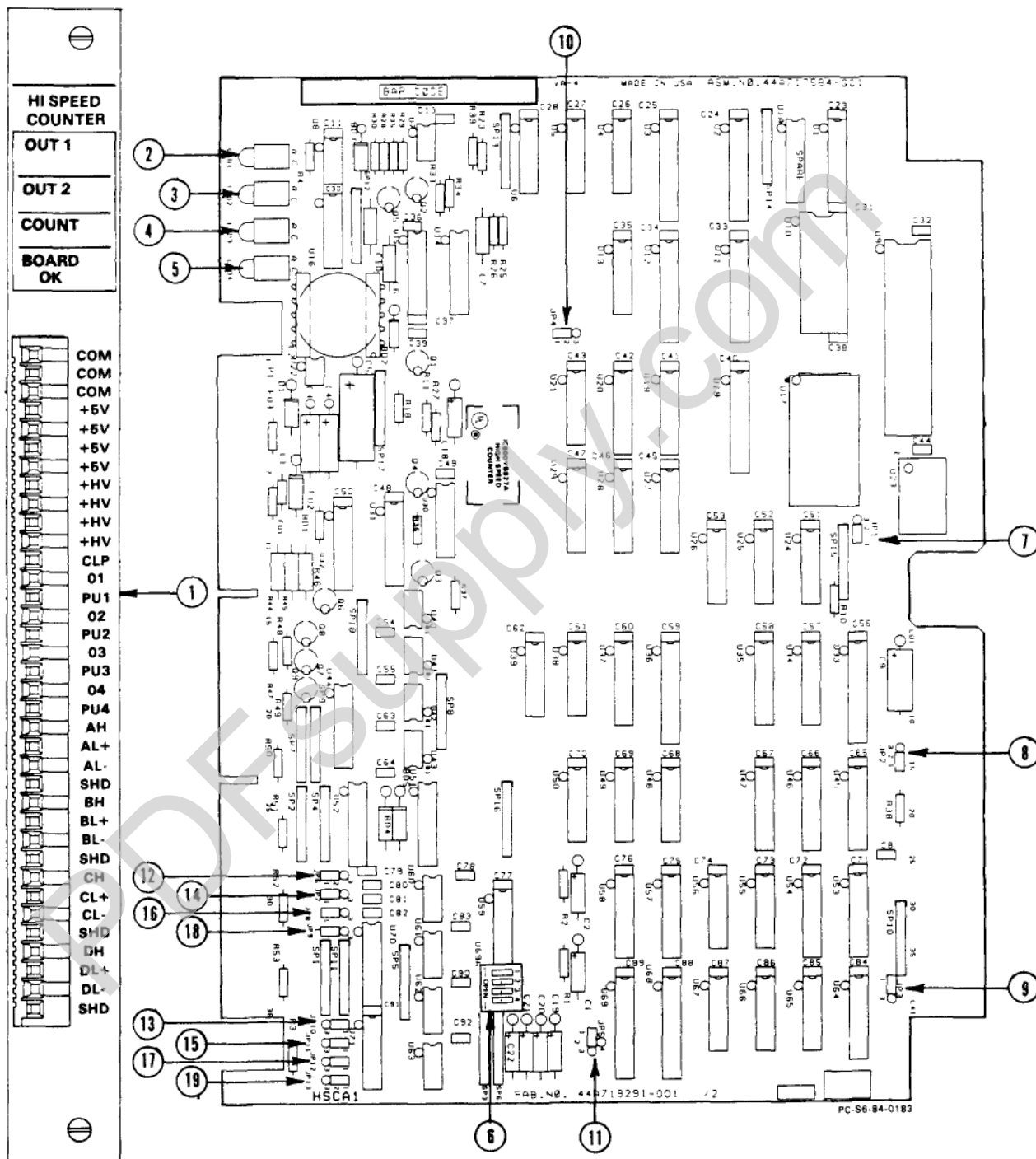


Figure 2. CONFIGURABLE USER SETTINGS (Part 1 of 3)

ITEM	FUNCTION FOR USER SETTINGS
①	Faceplate with lens and 36-point connector.
②	LED for OUT 1; when ON, indicates output 1 is energized.
③	LED for OUT 2; when ON, indicates output 2 is energized.
④	LED for count; when blinking, indicates pulses are being received.
⑤	LED for Board OK; when ON, Board passed diagnostic test.

ITEM	DIP SWITCH	FUNCTION					
6	SW1 Open* SW2 Open* SW3 Open* SW4 Closed	<table border="0"> <tr> <td>Input A Filter</td> <td rowspan="4">} Switch Open: 100 Hz Filter Disabled Switch Closed: 100 Hz Filter Enabled</td> </tr> <tr> <td>Input B Filter</td> </tr> <tr> <td>Input C Filter</td> </tr> <tr> <td>Input D Filter</td> </tr> </table> <p>Set to Closed position if input is connected to a device using dry contacts, or other non-solid state device.</p>	Input A Filter	} Switch Open: 100 Hz Filter Disabled Switch Closed: 100 Hz Filter Enabled	Input B Filter	Input C Filter	Input D Filter
Input A Filter	} Switch Open: 100 Hz Filter Disabled Switch Closed: 100 Hz Filter Enabled						
Input B Filter							
Input C Filter							
Input D Filter							

ITEM	JUMPERS	FUNCTION FOR USER SETTINGS
7	JP1 1-2* 2-3	<p>Run - Normal Use Factory Test</p>
8	JP2 1-2* 2-3	<p>If the CPU RESET signal is high, the counter will continue to function, except outputs 1 thru 4 will be forced off regardless of their previous state. When the CPU once again becomes operational, the four outputs will return to their conditional state as determined by the enable/disable and latch/unlatch bits and the preset comparison state.</p> <p>If the CPU RESET signal is high, the counter will continue to function, and will retain full control over its four outputs.</p>
9	JP3 1-2* 2-3	<p>Not Used Not Used</p>

* Factory Setting

FIGURE 2. CONFIGURABLE USER SETTINGS (PART 2 OF 3)

<u>ITEM</u>	<u>DIP SWITCH</u>	<u>FUNCTION</u>
⑩	JP4	
	1-2*	Encoder mode - Quadrature Encoder with optional marker
	2-3	Counter mode - Square wave pulse input
⑪	JP5	
	1-2*	X1 for quadrature encoder input
	2-4	X2 for quadrature encoder input
	2-3	X4 for quadrature encoder input
		Must be set to X1 when in counter mode
⑫⑬	JP6 JP10	
	1-2* 1-2*	Input A - 5V differential
	1-2 2-3	Input A - TTL single ended
	2-3 2-3	Input A - 10-30V single ended
⑭⑮	JP7 JP11	
	1-2* 1-2*	Input B - 5V differential
	1-2 2-3	Input B - TTL single ended
	2-3 2-3	Input B - 10-30V single ended
⑯⑰	JP8 JP12	
	1-2* 1-2*	Input C - 5V differential
	1-2 2-3	Input C - TTL single ended
	2-3 2-3	Input C - 10-30V single ended
⑱⑲	JP9 JP13	
	1-2 1-2	Input D - 5V differential
	1-2 2-3	Input D - TTL single ended
	2-3 2-3	Input D - 10-30V single ended

* Factory Setting

FIGURE 2. CONFIGURABLE USER SETTINGS (PART 3 OF 3)

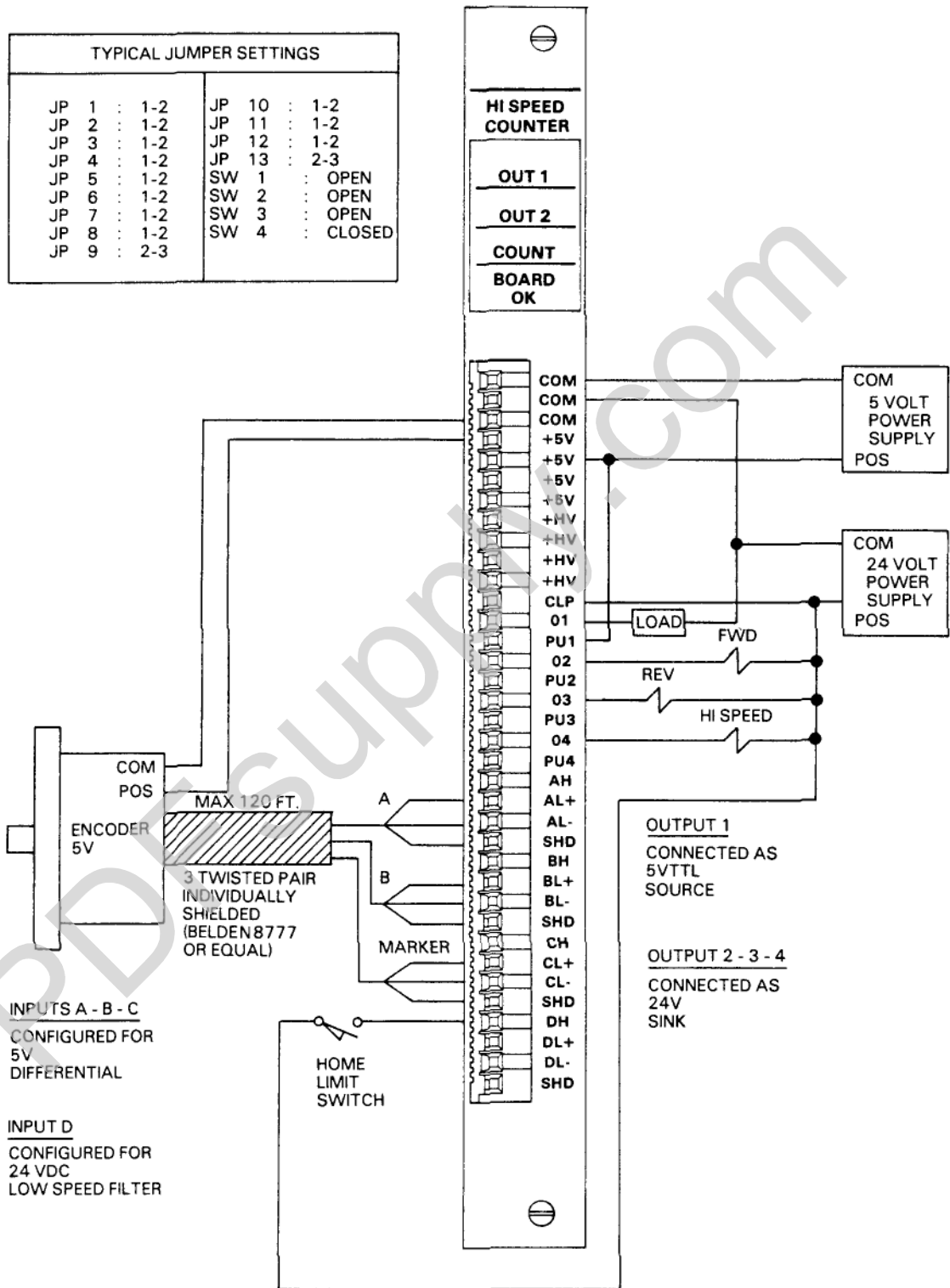


Figure 3. HIGH SPEED COUNTER - ENCODER MODE APPLIED TO CARRIAGE POSITION CONTROL

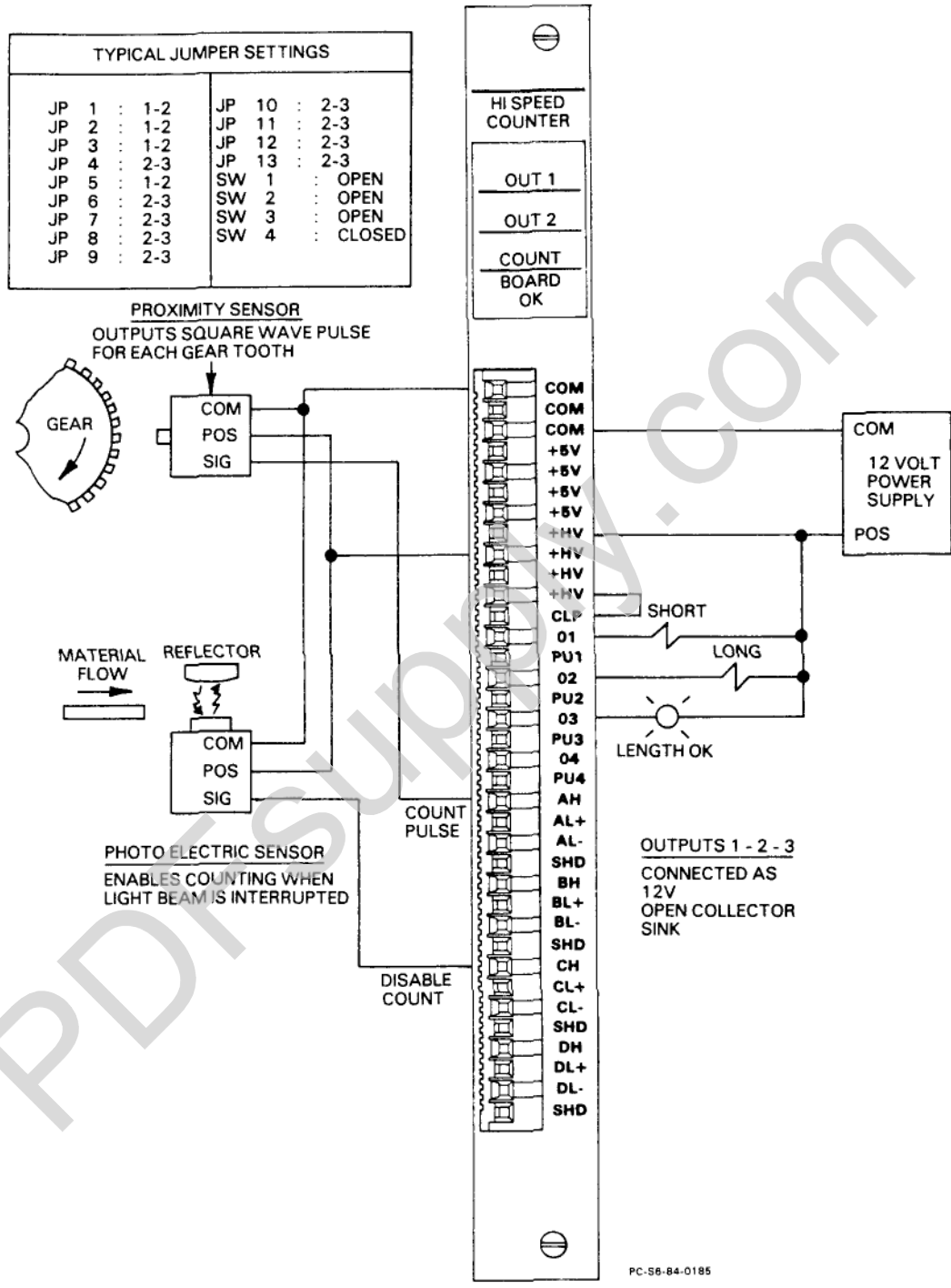


Figure 4. HIGH SPEED COUNTER - COUNTER MODE APPLIED TO LENGTH MEASUREMENT CONTROL

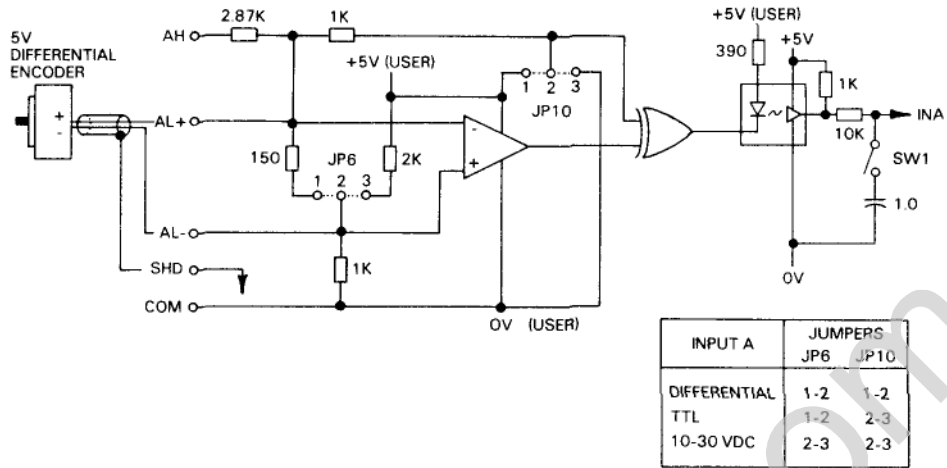


Figure 5. TYPICAL DIFFERENTIAL INPUT LOGIC DIAGRAM

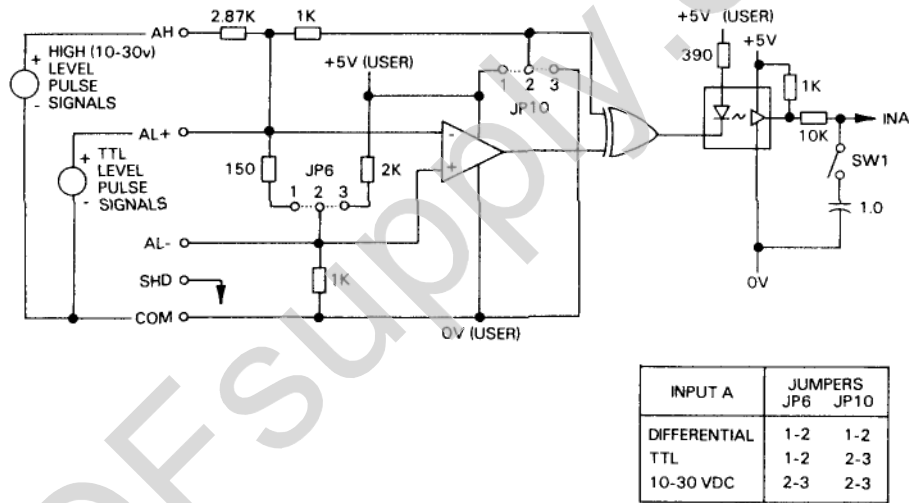


Figure 6. TYPICAL PULSE INPUT LOGIC DIAGRAM

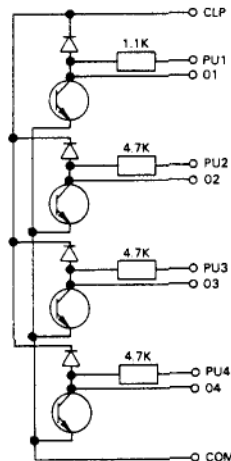


Figure 7. OUTPUT LOGIC DIAGRAM

HARDWARE INTERFACE

All external wiring connections to the High Speed counter module are made via the 36point terminal connector on the module faceplate. Table 3 details the function of each terminal point. Please note that all terminals with the same name (i.e. COM, + 5V, +HV, SHD) are internally

connected when the terminal strip is connected to the printed circuit board. If shielded cable is used, system earth ground is provided via faceplate to chassis connection and the grounding of the chassis enclosure. For typical wiring diagrams refer to Figure 3 and 4.

TABLE 3. TERMINAL WIRING DESCRIPTION

TERMINAL NUMBER	NAME	FUNCTION
1,2,3	COM	Common ground connection.
4,5,6,7	+5v	User power supply positive connection for 5V operation.
8, 9, 10, 11	+HV	User power supply positive connection for 10-30V operation.
12	CLP	Clamp diode connection. Protects outputs from inductive kick-back from the load. The CLP terminal should be jumpered to the positive side of the output power supply.
13 14	01 PUI	Open collector sink output. TTL compatible up to 50ma. Outputs can sink 250 ma. continuous, 500 ma. peak. The maximum supply voltage is 30V. If the PUI terminal is connected to the positive terminal of the output supply, the output will be pulled up through a 1100 ohm resistor. This output can drive the Series Six interrupt input board using a 24-30V power supply.
15 16	02 PU2	Open collector sink output. TTL compatible up to 50ma. Outputs can sink 250 ma. continuous, 500 ma. peak. The maximum supply voltage is 30 V. If the PU2 terminal is connected to the positive terminal of the output supply, the output will be pulled up through a 4700 ohm pull-up resistor.
17 18	03 PU3	Open collector sink output. TTL compatible up to 50 ma. Outputs can sink 250 ma. continuous, 500 ma. peak. The maximum supply voltage is 30V. If the PU3 terminal is connected to the positive terminal of the output supply, the output will be pulled up through a 4700 ohm pull-up resistor.
19 20	04 PU4	Open collector sink output. TTL compatible up to 50 ma. Outputs can sink 250 ma, continuous, 500 ma. peak. The maximum supply voltage is 30V. If the PU4 terminal is connected to the positive terminal of the output supply, the output will be pulled up through a 4700 ohm pull-up resistor.
21 22 23 24	AH AL+ AL- SHD	These terminals form the IN A input. The settings of JP6 and JP10 determine the input type (see Figure 2). In the COUNTER mode IN A is used for the incoming square wave pulses. In the ENCODER mode this input is used for quad A of the encoder.

TABLE 3. TERMINAL WIRING DESCRIPTION (CONTINUED)

TERMINAL NUMBER	NAME	FUNCTION
25 26 27 28	BH BL+ BL- SHD	<p>These terminals form the IN B input. The settings of JP7 and JPI 1 determine the input type (see Figure 2).</p> <p>In the COUNTER mode these terminals are used for the count direction control. With no signal applied the count direction is UP. If the direction is to be controlled via software, the input should be disabled, or not connected. Up/Down is controlled in software by bit 10 of the Discrete command (see Figure 9).</p> <p>In the ENCODER mode this input is used for quad B of the shaft encoder.</p>
29 30 31 32	CH CL+ CL- SHD	<p>These terminals form the IN C input. The settings of JP8 and JP12 determine the input type (see Figure 2).</p> <p>In the COUNTER mode these terminals are used as a counter enable control. With no signal applied the counter is ENABLED. If the counter enable is to be controlled by software command, IN C should be disabled, or not connected. Enable/Disable is controlled in software by Bit 9 of the Discrete Command (see Figure 9).</p> <p>In the ENCODER mode this input is used for the marker pulse of the shaft encoder. If there is no marker present then no connection should be made to this input.</p>
33 34 35 36	DH DL+ DL- SHD	<p>These terminals form the IN D input. The settings of JP9 and JP13 determine the input type (see Figure 2).</p> <p>In the COUNTER mode the IN D input is used to reset the counter. The reset function forces the accumulated count to the Lower Count Limit. The reset condition will exist as long as the IN D signal is asserted. With no signal applied the counter is NOT RESET. The count can also be reset by software command. IN D should be disabled or not connected if software control is used. Reset is controlled in software by Bit 19 of the Discrete Command (see Figure 9).</p> <p>In the ENCODER mode the IN D input is used to establish home position. When the HOME command is active and the IN D limit switch is asserted, the next marker pulse will cause the accumulated count to be set to the home position value. After the marker occurs, incoming pulses will be counted, and will represent an offset from HOME position.</p>

GENERAL DESCRIPTION OF OPERATION

The intelligent High Speed Counter module receives command data from the Series Six CPU logic program and returns count and status data to the CPU. These data transfers requires 32 input and 32 output points. There are also four input circuits and four output circuits for connection to field devices. Refer to Table 3 for a full description of each.

The High Speed Counter card has two basic modes of operation (counter or encoder) which are selectable by means of a jumper. The functions of the inputs depends on the mode of operation selected.

In the Counter mode the inputs are defined as follows:

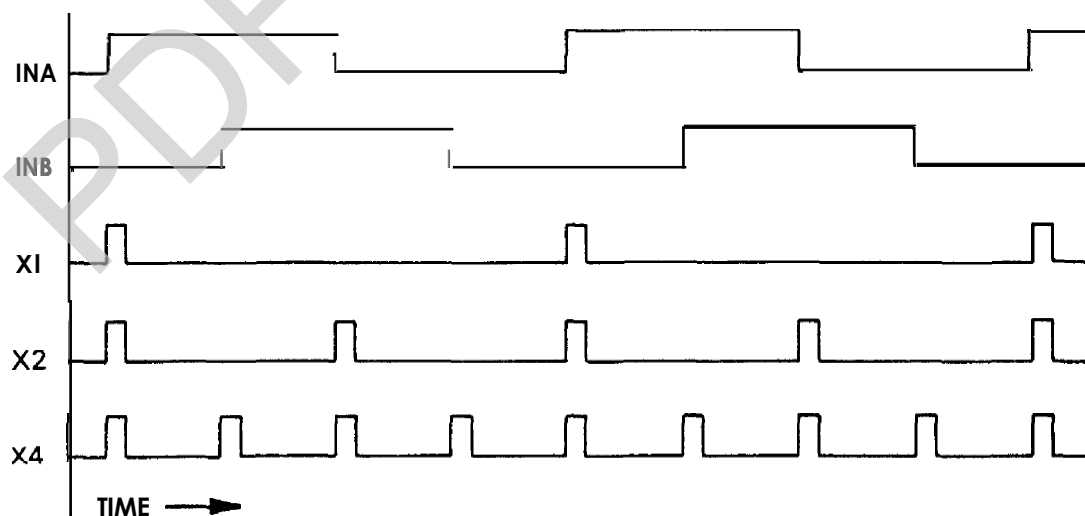
- INA Pulse Input: connected to the pulses to be counted.
- INB Direction Input: controls the direction of counting.
- INC Enable/Disable Input: used to enable or disable counting.
- IND Reset Input: sets the Accumulate register to the Lower Count Limit and inhibits counting while active.

In the Encoder mode the inputs have the following meanings:

- INA Quad A Input: connected to channel A of the quadrature encoder.
- INB Quad B Input: connected to channel B of the quadrature encoder.
- INC Marker Input: connected to the marker channel of the encoder.
- IND Limit Switch Input: used to establish True Home Position.

Each input is provided with a selectable filtering network. When the filter is selected, the frequency response of the input is limited to 100Hz (square wave). The filter is normally used for debouncing mechanical contacts.

When the ENCODER mode is selected, one of three counting rates: X1, X2, or X4 can be jumper selected by the user. When the COUNTER mode is selected, the jumper must be placed in the X1 position. Figure 8 shows the effect of this jumper selection for when quadrature encoders are used.



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FIGURE 8. QUADRATURE PULSE COUNTING

The module contains an 8 bit counter which is read by the counter software and used to maintain a 24 bit Accumulate register. The counting range of this register is -8,388,608 to +8,388,607. Negative values are kept as 2's complement. The user can define the upper and lower counting limits anywhere within this range (the Upper Count Limit minus the Lower Count Limit must be greater than 128). When counting up, the Accumulate register will be set to the Lower Count Limit after reaching the Upper Count Limit plus one. When counting down, the Accumulate register will be set to the Upper Count Limit when reaching the Lower Count Limit minus one.

The four outputs are open collector transistors which can provide TTL compatible levels. Individual pull-up resistors are provided to allow outputs to drive TTL or CMOS logic without the use of external resistors. When used in the open collector configuration, the outputs can sink 250 ma. of current and can accept up to 30V. The output circuitry is optically isolated and detailed in Figure 7.

The state of each of the four outputs is determined by a combination of five factors:

1. Preset/Accumulate Relationship (< , ≥)
2. Comparison Sense (Command # 35)
3. Disable/ Enable (Discrete Command)
4. Unlatch/Latch (Discrete Command)
5. Previous State of Output

How these factors control an output is shown in Table 4.

NOTE

Once an output has been turned on through the conditions described in Table 4, it can be latched on using discrete commands 15-18 (Refer to Figure 9). Once an output is latched on it will remain on regardless of changes in the Disable/Enable or Preset Comparison function. The output will not be turned off until it is unlatched, and the conditions in Table 4 are appropriate.

TABLE 4. OUTPUT STATE TABLE

Accumulate <, ≥ Preset	Comparison Sense (CMMD # 35)	Preset* Comparison Function	Disable/ Enable	output State
^ W ^ W	0	0	0	0
	0	1	0	0
	0	0	1	0
	0	1	1	1
^ W ^ W	1	1	0	0
	1	0	0	0
	1	1	1	1
	1	0	1	0

Result of Preset Comparison is determined by the comparison sense (Command # 35), and the Preset/Accumulate relationship (<, ≥).

When configured for open collector operation, outputs can be paralleled. In conjunction with the preset compare and enable/disable functions, custom ON/OFF switching patterns can be established. It should be noted that the counter does not monitor the state of the outputs. Therefore, if a failure in that circuitry should occur, the CPU delete "system" will not be aware of it.

In addition to the four outputs, the counter module provides eight programmable Internal Preset registers. CPU logic can download preset limits which are then compared to the accumulated count with the resultant state (true or false) returned to the CPU.

Because the counter is an intelligent module, it is capable of continued operation regardless of the operating state of the CPU. This feature is selectable via a jumper and is conditioned upon the module being previously downloaded with preset data from the CPU and the I/O rack and external power supplies being operational.

An external user-furnished power supply is required to support the delete "field" isolated Input and Output logic. The power supply may be 5 VDC or 10-30 VDC. If this, or the rack power supply should lose power, the module must be reloaded from the CPU. An appropriate status bit will be set.

CPU INTERFACE

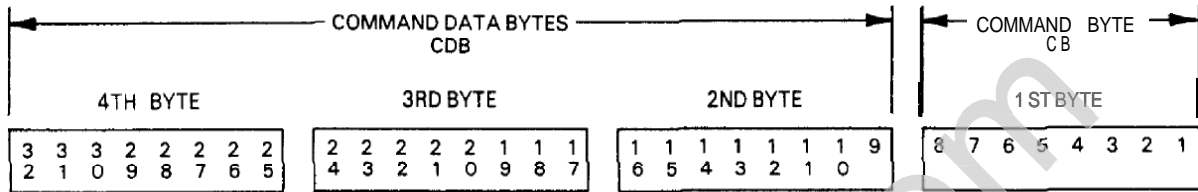
Communications between the High Speed Counter module and the Central Processor Unit (CPU) is accomplished via 32 consecutive input and output bits. (I/O address selection is discussed under Installation.) Command and preset data is transferred from the CPU to the counter module, while board status, output status, accumulated count, or counts/time-base is returned from the counter to the CPU. A two way data transfer will occur with every CPU I/O scan.

Since data is only transferred between the CPU and the counter in the I/O scan, the user needs to consider carefully the use of the Suspend I/O instruction. The counter will continue operation without communication to the CPU when the I/O is suspended, but it will not be able to apprise the CPU of its status. In similar context, use of the DO I/O instruction, which could poll the counter too frequently, would tend to cause the module to respond slowly to the degree that it may miss a pulse. To prevent this, a minimum of 6 msec should elapse between I/O scans that use the I/O addresses of the counter.

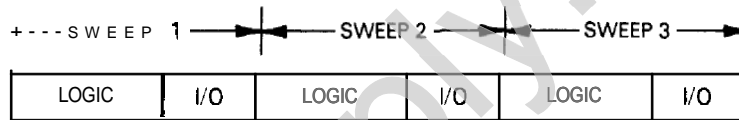
DATA SENT FROM SERIES SIX CPU

The first 8 bits or the first byte of data transferred from the CPU to the counter is referred to as the Command Byte (CB), while the remaining 24 bits or 3 bytes are

referred to as the Command Data Bytes. This data uses 32 bits of the CPU output table.



Information contained in the Command Data Bytes is interpreted by the counter based upon the Command Number contained in the Command Byte.



- If the CPU issues a command in Sweep 1 that requires a specific type of data to be returned, that data will be returned in Sweep 2, and be available for logic solutions in Sweep 3.
- If a command is issued that does not request return data, the previously requested data will continue to be returned.
- If a command generates an error, that Error Code will be returned in the next I/O sweep. Subsequent sweeps will return data that was previously requested.
- A CPU SUSPEND I/O function will stop all communications to the counter module while allowing it to continue in full operation.
- A CPU DO I/O function, which addresses a specific counter, can be used to download system parameters. However, communications with the counter must not occur more often than every 6 milliseconds.

COMMAND BYTE (CB)

The Command Byte contains a Command Number that is used to set up the operational characteristics of the High Speed Counter. CPU logic selects the Command Number to be executed in the counter module and places that number in the Command Byte. One command is executed

per I/O scan. Once card set up is complete, the Command Number is usually set to zero. The Command Data Bytes contain the information necessary to complete the execution of the command specified. Table 5 contains a list of all the commands along with a detailed description.

TABLE 5, COMMAND NUMBER

COMMAND NUMBER		DEFINITION OF COMMAND
DECIMAL VALUE	HEX VALUE	
0	00	DISCRETE COMMANDS - Interpret data bits (9-32) as discrete commands as detailed in Figure 9.
1	01	RESET CARD - Accumulated count and preset register are set to zero; outputs are turned off and board returned to initial default conditions, diagnostic tests are run, if tests are passed, the heartbeat will toggle and the Power-Up Bit of the Status Byte will be set; all commands except the Reset Card command will be ignored until this Power-Up Bit is cleared by Command 6. If the diagnostic tests fail an error code will be returned on the next I/O scan and the Board OK LED is turned off.
2	02	CONTINUE - This is a null command and the counter will continue to operate in the previously commanded mode. When used, this command improves counter processing time.
3	03	RETURN DISCRETE COMMAND - Return data bits (9-32) of Last Discrete Command (CB =0) sent as detailed in Figure 11.
4	04	HOME POSITION - Used only in encoder mode. (Refer to Figure 13.) Data bytes will contain value of Home Position location, all outputs are disabled and unlatched, the Home Position Bit in the returned Status Byte is cleared and incoming count pulses are ignored, On first Marker Pulse (Input C) after Home Limit Switch signal (Input D) is received: Home Position value is loaded into accumulate register, incoming pulses will ADD/SUBTRACT from accumulate register to track offset from Home Position, Home Position bit (SB=5) is set, and outputs remain disabled. If, in Encoder Mode, Home Position Value is outside the Upper or Lower Count Limit, or if another command is issued while the Home Command Bit is set, an error code will be returned. This command is active until Home Position is found or Abort Home Position (CB=5) or Reset Card (CB= 1) is issued.
5	05	ABORT HOME POSITION COMMAND - Used only in Encoder Mode; cancels Command 4; count pulses are again accepted while outputs are held disabled. Outputs must be re-enabled via the Discrete Command (CB =0). Since Home Position was not established and counting was disabled, the Accumulate Register value should be used with caution. If not in the Counter Mode or if the Home Position (Command 4) is not active, an error code will be returned.
6	06	CLEAR POWER-UP BIT - Sets Bit 2 of Status Byte to zero; this bit must equal zero for the counter module to accept any command other than Reset Card (CB= 1); bit will be set on power-up, external power supply failure, or after Reset Card command is issued.
7 thru 15	07 thru 0F	Reserved for future use.

TABLE 5. COMMAND NUMBER (CONTINUED)

COMMAND NUMBER		DEFINITION OF COMMAND
DECIMAL VALUE	HEX VALUE	
16	10	LOAD OUTPUT 1 PRESET REGISTER from Command Data Bytes
17	11	LOAD OUTPUT 2 PRESET REGISTER from Command Data Bytes
18	12	LOAD OUTPUT 3 PRESET REGISTER from Command Data Bytes
19	13	LOAD OUTPUT 4 PRESET REGISTER from Command Data Bytes
20	14	LOAD INTERNAL PRESET REGISTER 1 from Command Data Bytes
21	15	LOAD INTERNAL PRESET REGISTER 2 from Command Data Bytes
22	16	LOAD INTERNAL PRESET REGISTER 3 from Command Data Bytes
23	17	LOAD INTERNAL PRESET REGISTER 4 from Command Data Bytes
24	18	LOAD INTERNAL PRESET REGISTER 5 from Command Data Bytes
25	19	LOAD INTERNAL PRESET REGISTER 6 from Command Data Bytes
26	1A	LOAD INTERNAL PRESET REGISTER 7 from Command Data Bytes
27	1B	LOAD INTERNAL PRESET REGISTER 8 from Command Data Bytes

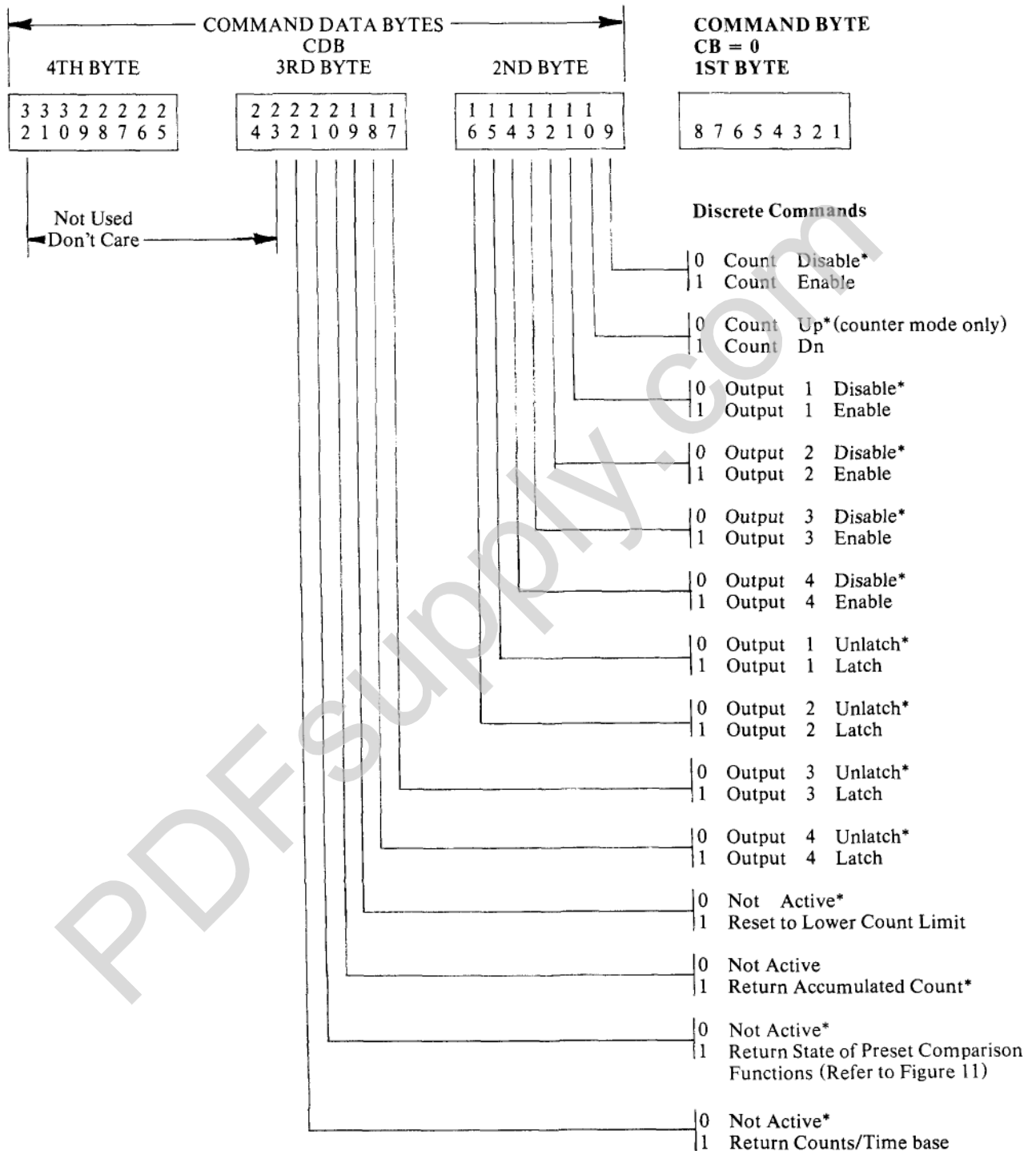
If Preset Value is above the Upper Count Limit or below the Lower Count Limit, an error code will be returned and, the command will not be executed. Counter operation remains unchanged. Default value upon power-up is zero.

TABLE 5. COMMAND NUMBERS (CONTINUED)

COMMAND NUMBER		DEFINITION OF COMMAND
DECIMAL VALUE	HEX VALUE	
28 thru 31	1C thru 1F	Reserved for future use.
32	20	LOAD ACCUMULATE REGISTER from Command Data Bytes-If new Accumulate Value is above the Upper Count Limit or below the Lower Count Limit, an error code will be returned and, the command will not be executed. Counter operation remains unchanged, Default value upon power-up is zero.
33	21	LOAD UPPER COUNT LIMIT from Command Data Bytes-If Upper Count Limit minus the Lower Count Limit is less than 128, an error code will be returned and, the command will not be executed. Counter operation remains unchanged. Default value upon power-up is 8,388,607 or 7FFFFFFF(HEX).
34	22	LOAD LOWER COUNT LIMIT from Command Data Bytes-If Upper Count Limit minus the Lower Count Limit is less than 128, an error code will be returned and, the command will not be executed. Counter operation remains unchanged. Default value upon power-up is zero. Lower count limit is -8,388,608 or 800000 (HEX).
35	23	LOAD PRESET COMPARISON SENSE - Interpret Command Data Bytes (bits 9-32) as detailed in Figure 10.
36	24	LOAD TIME BASE from Command Data Bytes- Sets time base in milliseconds for measurement of count pulses/ time base for use in velocity feedback. If time base is set outside of range 1 to 65,535 (milliseconds), an error code will be returned and, the command will not be executed. Counter operation remains unchanged.
37 thru 47	25 thru 2F	Reserved for future use.

TABLE 5. COMMAND NUMBERS (CONTINUED)

COMMAND NUMBER		DEFINITION OF COMMAND
DECIMAL VALUE	HEX VALUE	
48	30	RETURN OUTPUT 1 PRESET REGISTER
49	31	RETURN OUTPUT 2 PRESET REGISTER
50	32	RETURN OUTPUT 3 PRESET REGISTER
51	33	RETURN OUTPUT 4 PRESET REGISTER
52	34	RETURN INTERNAL PRESET REGISTER 1
53	35	RETURN INTERNAL PRESET REGISTER 2
54	36	RETURN INTERNAL PRESET REGISTER 3
55	37	RETURN INTERNAL PRESET REGISTER 4
56	38	RETURN INTERNAL PRESET REGISTER 5
57	39	RETURN INTERNAL PRESET REGISTER 6
58	3A	RETURN INTERNAL PRESET REGISTER 7
59	3B	RETURN INTERNAL PRESET REGISTER 8
60 thru 63	3c thru 3F	Reserved for Future Use
64	40	RETURN ACCUMULATE REGISTER (CB = 32)
65	41	RETURN UPPER COUNT LIMIT (CB=33)
66	42	RETURN LOWER COUNT LIMIT (CB=34)
67	43	RETURN PRESET COMPARISON SENSE (CB=35)
68	44	RETURN TIME BASE (CB=36)
69 thru 255	45 thru 7F	Reserved for future use

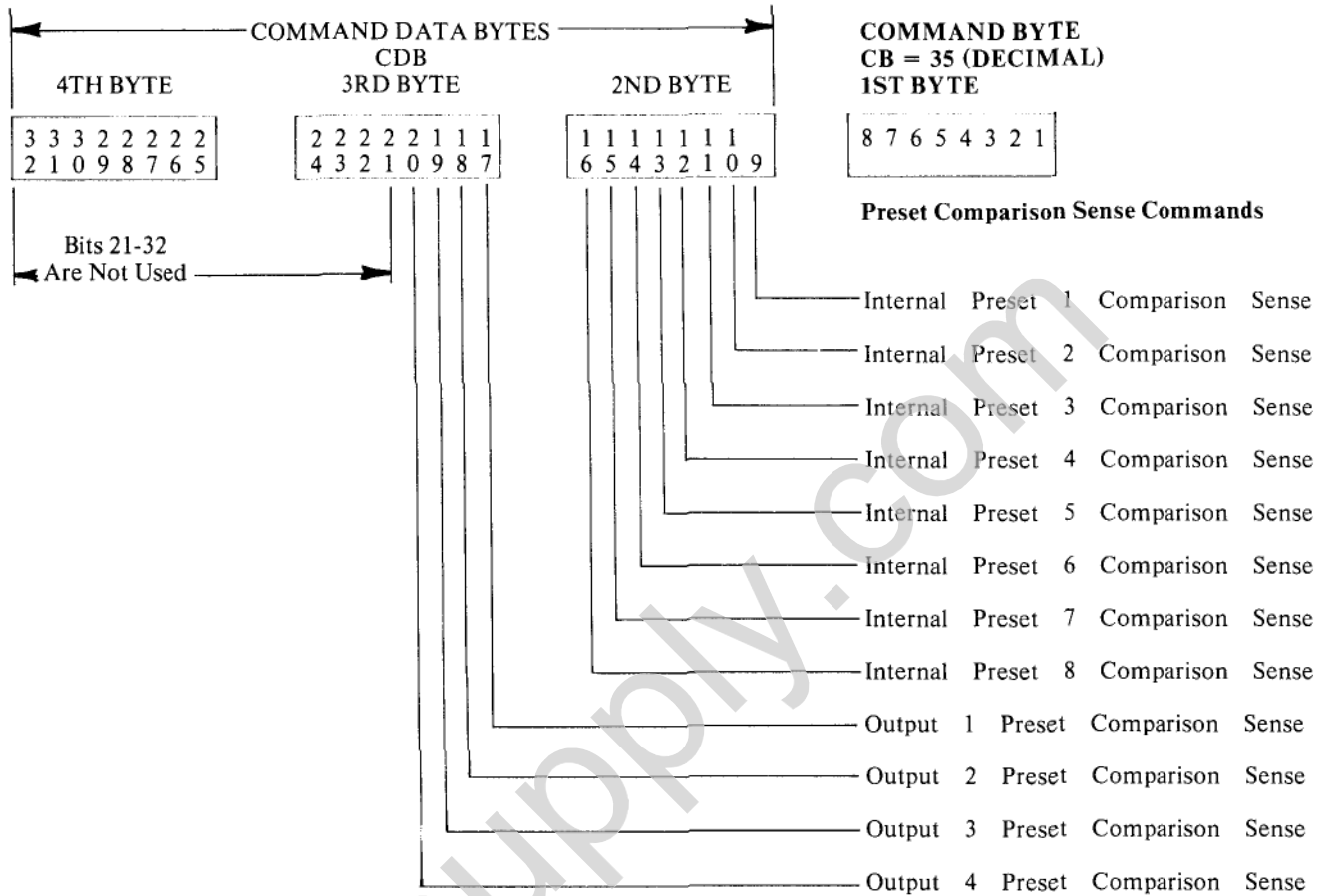


* Default conditions on power-up

NOTE

The High Speed Counter will interrupt and act upon each bit every time this data set is received from the CPU. The module will execute, for function bits 20, 21, 22 only, the lowest bit number function if more than one bit is set.

Figure 9. DISCRETE COMMAND FORMAT
 COMMAND BYTE EQUALS ZERO (CB=0)



NOTE

The Load Preset Comparison Sense command (CB = 35) establishes the True, False (1/0) comparison sense between the accumulate and the twelve presents in the counter module. Output # 9 through # 20 set the sense for the eight internal and four output presets. If the output is off (0), the respective preset comparison function will be true (1) when the accumulated count is greater than or equal (\geq) to the preset. If the output is on (1), the preset comparison function will be true when the accumulated count is less than ($<$) the preset. The following chart illustrates this concept.

Figure 10. PRESET COMPARISON SENSE

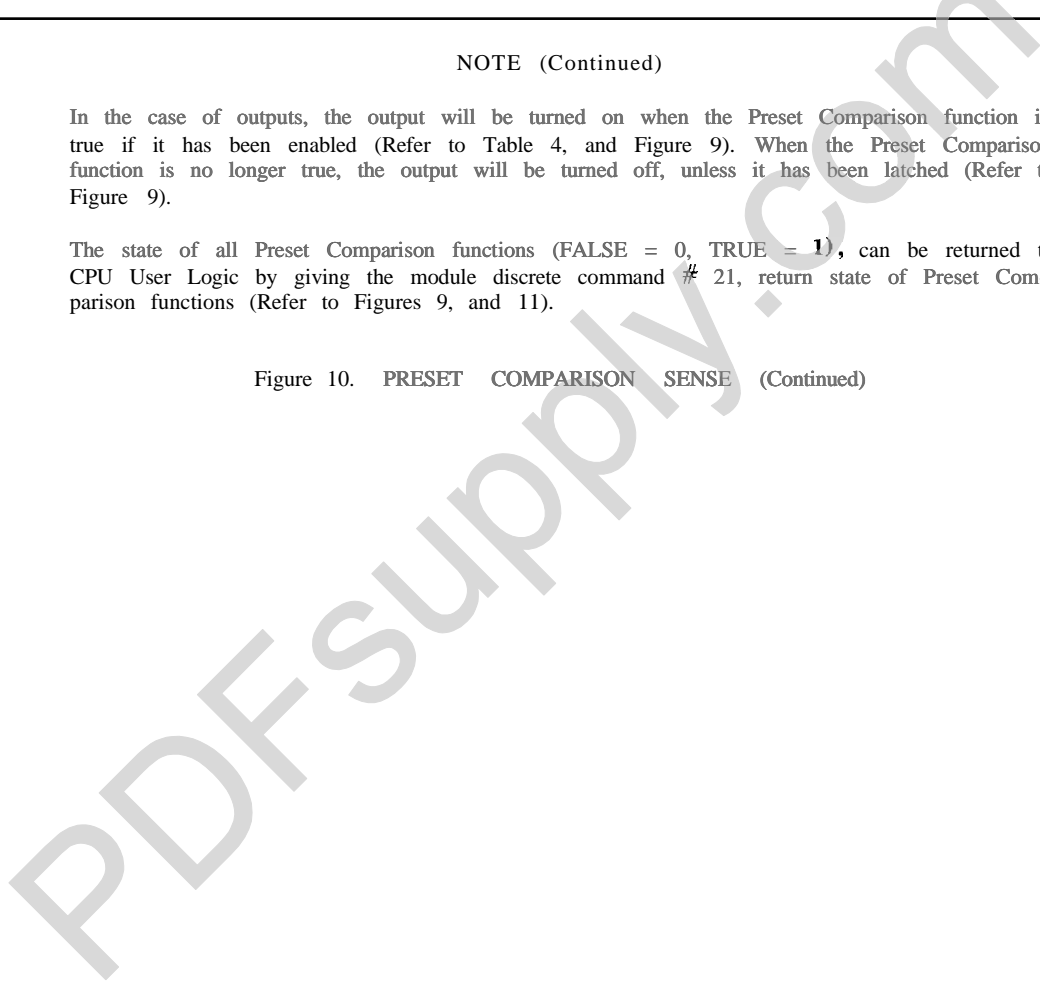
ACCUMULATED <, PRESET	COUNT	COMPARISON SENSE	PRESET COMPARISON FUNCTION
<		OFF (0)	FALSE (0)
≧		OFF (0)	TRUE (1)
<	3	ON (1)	TRUE (1)
3		ON (1)	FALSE (0)

NOTE (Continued)

In the case of outputs, the output will be turned on when the Preset Comparison function is true if it has been enabled (Refer to Table 4, and Figure 9). When the Preset Comparison function is no longer true, the output will be turned off, unless it has been latched (Refer to Figure 9).

The state of all Preset Comparison functions (FALSE = 0, TRUE = 1), can be returned to CPU User Logic by giving the module discrete command # 21, return state of Preset Comparison functions (Refer to Figures 9, and 11).

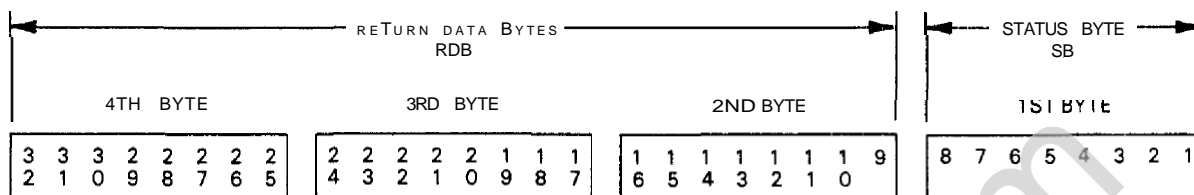
Figure 10. PRESET COMPARISON SENSE (Continued)



DATA RETURNED TO SERIES SIX CPU

The first 8 bits, or the first byte of data, transferred to the CPU from the counter is referred to as the Status Byte, while the remaining 24 bits or 3 bytes are referred to as

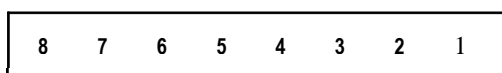
the Returned Data Bytes. This data uses 32 bits of the CPU Input Table.



Information contained in the Returned Data Bytes is that data which was requested via the Command Number contained in the Command Byte issued during the previous I/O scan. The previously requested data type will be returned every I/O scan unless a new type of return data is requested. Default returned data on power-up is the accumulated count value.

All commands (except Reset Card) will be ignored until the Power-Up bit is reset to a zero (0) by the Clear Power-up Bit Command (CB = 6).

STATUS BYTE



1st BYTE

Bit 4 - COUNTING ENABLED: This bit, when set to a one (1) by the counter module, indicates that the counter is enabled. The Count Enable command (CB=0, bit 9) must be set to one (1) to enable counting. To Disable counting, set bit 9 to zero (0), or in the Count Mode, apply a signal to Input C.

The Status Byte (SB) contains information pertaining to the current operating status of the High Speed Counter. This byte is updated and returned to the CPU every I/O scan. Definition of the Status Byte bits is as follows.

Bit 5 - HOME/DIRECTION: In the Encoder Mode this bit indicates that Home Position has been established, and is set to a one (1) when any of the following events occur:

Bit 1 - HEARTBEAT: This bit indicates if the board is functional. It is toggled every time an I/O scan occurs except during power-up diagnostics. Any failures of counter diagnostics will stop the heartbeat.

- a. After the Home Command (CB=4) is issued, and the first Marker Pulse is received after the Home Limit Switch is reached. Refer to Figure 14.
- b. A load Accumulate command (CB=32) is issued.
- c. A Reset Accumulate to Lower Count Limit (CB=0, bit 19) is issued.

Bit 2 - POWER-UP: This bit is set by the module to a one (1) whenever rack or external power is applied, either for the first time or following a power dip. On power-up, the counter will run its diagnostic tests and reset all internal data registers to their default values.

This bit is reset to zero (0) on Power-up, Reset Command (CB=0), or Home Command (CB=4).

A Reset Card Command (CB= 1) from the CPU will also cause diagnostics to be executed and the Power-Up bit to be set.

In the Counter Mode this bit indicates the direction of count (0 = up, 1 = down). Direction is a function of Input B or the Up/Down Count command (CB=0, bit 10). Count direction is Up unless a signal is applied to Input B or CB=0, bit 10 is set to a one (1).

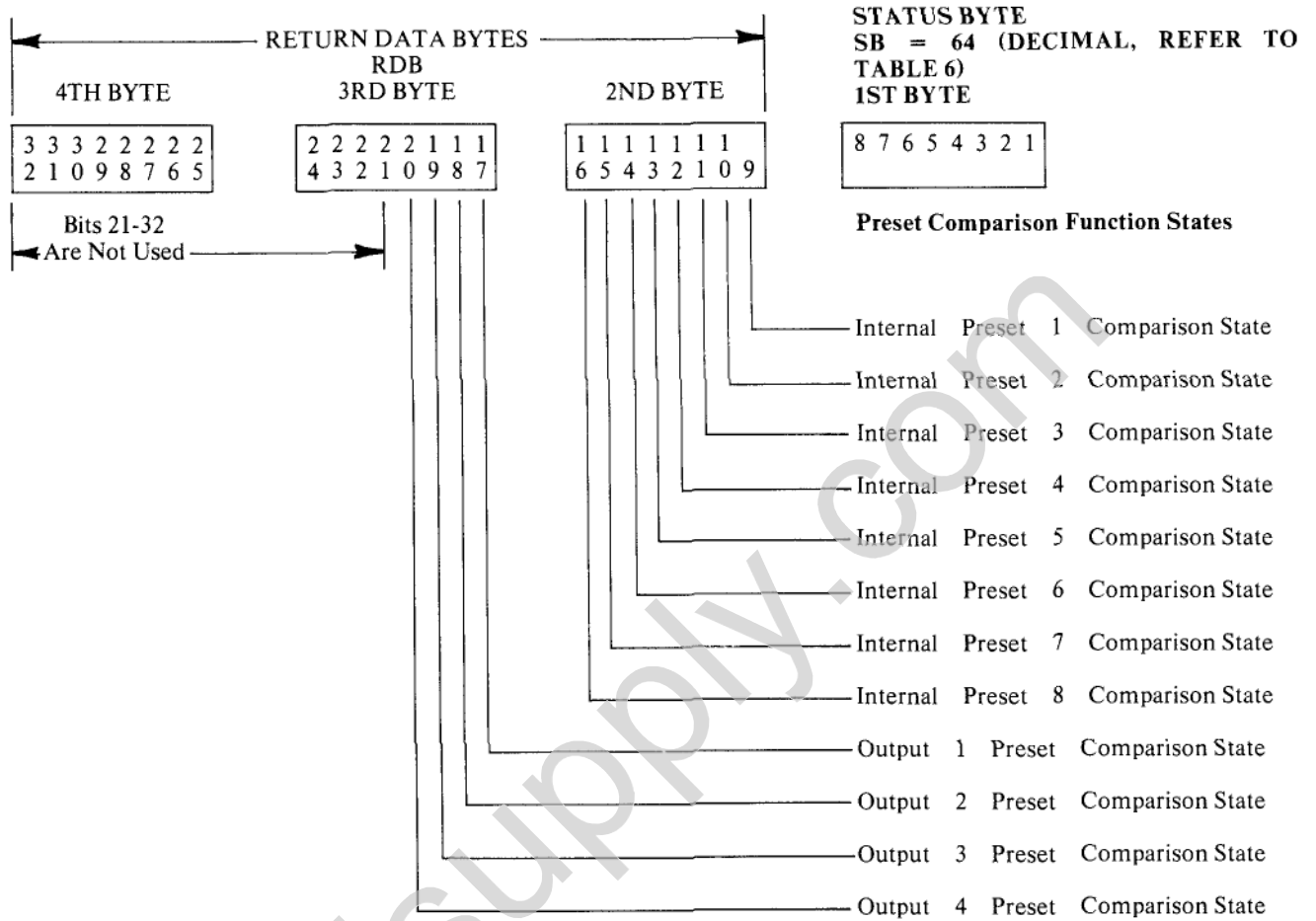
All commands (except Reset Card) will be ignored until this bit is reset to zero (0) by the Clear Power-up Bit Command (CB - 6).

Bits 6, 7, 8 - Returned Data Type: Interpretation of these bits indicates the type of data being returned to the CPU in the Return Data Bytes 2, 3, and 4. If an error code is returned, the command that caused the error is ignored, and count operation remains unchanged. (Refer to Table 6)

Bit 3 - EXTERNAL POWER SUPPLY STATUS: This bit is set to a one (1) whenever the external (user) power supply is below 4.5V. When external power fails, the Power-Up bit is set and the counter will run its diagnostic tests and reset all data registers to their default values.

TABLE 6. RETURNED DATA TYPE

Bit 8	Bit 7	Bit 6	Data Returned
0	0	0	Accumulated Count (default on power-up)
0	0	1	Counts/Time base
0	1	0	Comparison States for Presets (see Figure 12)
0	1	1	Returned Data as requested in previous I/O scan from commands 3,48-59, 65-68
1	0	0	Error Code (see Figure 13)
1	0	1	Future Use
1	1	0	Future Use
1	1	1	Future Use



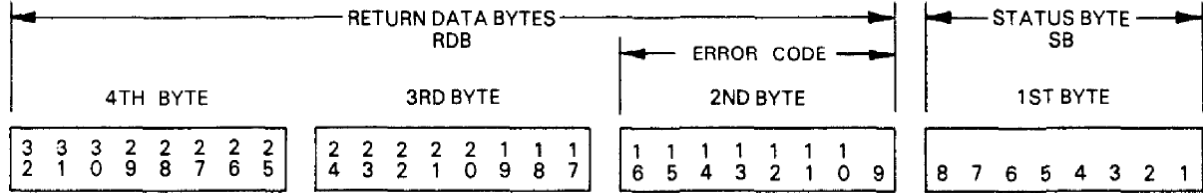
NOTE

This discrete data is returned to the CPU Input Table two sweeps after discrete command # 21 has been issued (Refer to Figure 9). Inputs 9 through 20 reflect the state of all Preset Comparison functions (Refer to Figure 10). If the Input is on (1), the Preset Comparison function is True. Conversely, if the Input is off (0), the Preset Comparison Function is False.

The state (ON/OFF) of each of the four outputs does not necessarily match the state of the Preset Comparison function. The Enable/Disable Latch/Unlatch, along with the Preset Comparison Function determine the ON/OFF status of each output (Refer to Table 4, and Figure 9).

Figure 11. COMPARISON STATES FOR PRESETS

ERROR CODES



When the Status Byte bits 6, 7, 8 indicate an error code is present (refer to Table 6), a binary number will be returned in the 2nd Byte indicating the particular Error Code. If a command generates an error, that command will be ignored and an Error Code will be present in the Return Data Bytes of the next I/O scan. Subsequent

sweeps will return the previously requested data. Counter operation remains unchanged from its current operating mode whenever an error code is sensed. The data contained in the 3rd and 4th bytes is indeterminate. The Error Codes are as follows.

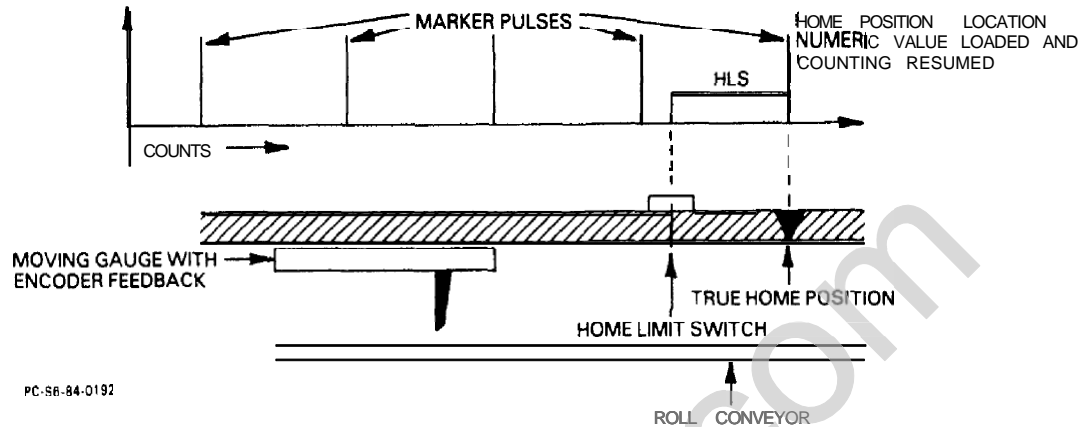
HIGH SPEED COUNTER ERROR CODES

DECIMAL VALUE	HEX VALUE	DESCRIPTION OF ERROR
1	1	Invalid Home Position value - The valid Home Position value should be: $LCL < = \text{Home Position} < = UCL$ LCL - Lower Count Limit UCL = Upper Count Limit The command was not executed.
2	2	Invalid Home Command - While in Home Position mode no commands are accepted. This error code will be generated if another Home command is issued before Home position is achieved.
3	3	Invalid Home Command - Home command was issued while in counter mode.
4	4	Invalid Abort Home Command - Abort Home command was not executed because card is not in Home Position Mode, or Home position has already been established.
5	5	Invalid Abort Home Command - Abort Home command was issued while in counter mode.
6	6	Invalid Command Number - Command does not exist.
7- 10	I - A	Invalid Output (1-4) Preset Value - Valid preset values are: $LCL < - \text{Output (1-4) Preset} < = UCL$ The command was not executed.

FIGURE 12. ERROR CODES

DECIMAL VALUE	HEX VALUE	DESCRIPTION OF ERROR
11-18	B-12	Invalid Internal Preset (1-8) Value - Internal Preset Value must lie between lower count limit and upper count limit, LCL \leq Internal Preset \leq UCL The command was not executed.
19	13	Invalid Accumulate Value - Valid Accumulate values are: LCL < = Accumulate < - UCL The command was not executed.
20	14	Invalid Upper Count Limit - Upper Count Limit minus Lower Count Limit should be greater than or equal to 128. The command was not executed.
21	15	Invalid Lower Count Limit - Upper Count Limit minus Lower Count Limit should be greater than or equal to 127. The command was not executed.
22	16	Invalid Time Base Value - Valid Time Base values are: 1 < = Time Base < = 65535
23	17	Invalid Command; Power-up Bit Set - When the power-up bit (bit 2 of the Status Byte) is set, the only commands the card will respond to are the Clear Power-up Bit command and the Reset Card command. The command was not executed.
24	18	Diagnostic Failure* - Internal RAM test failed. After error is sent heartbeat will die. Cycle power to reset this bit,
25	19	Diagnostic Failure* - External RAM failed. After error is sent heartbeat will die. Cycle power to reset this bit.
26	1A	Diagnostic Failure* - EPROM test failed. After error is sent heartbeat will die. Must re-cycle power.
27	1B	External Power Supply Failure - External power supply has gone out of tolerance. Card will go through power-up sequence, and all default conditions will be restored. * If the High Speed Counter fails to pass its self-diagnostic tests, reseal the module in the I/O rack and check power supplies. If the module does not respond properly replace it and return the failed unit to G.E. for repairs or call our Service Number 804-978-5747.

FIGURE 12. ERROR CODES (CONTINUED)



1. Set counter in Home Position Mode (CB=4). The Data Bytes will contain the numeric value of the Home Position Location. Counter outputs are turned off and incoming count pulses are ignored.
2. Advance gauge towards the home position.
3. When the Home Limit Switch is tripped, a signal is received at Input D.

The next Marker Pulse (Input C) from the Encoder C) marks the True Home Position.

4. The numeric value of the Home Position Location is now loaded into the Accumulate Register and counting resumed to track offset from the True Home Position. The outputs remain disabled and must be re-enabled by the CPU program.

FIGURE 13. HOME POSITION APPLICATION

DATA DOWNLOAD USING THE REGISTER TABLE

INTRODUCTION

Since the High Speed Counter Module is capable of counting high frequency input pulses it can be used in applications involving quadrature encoders and high speed digital tachometers and photosensors. The applications include cam switch simulations, velocity measurement applications, and position tracking applications. However, before the HSC can be utilized in any application the Series Six CPU must tell the counter via command data how and when to react to the incoming pulses.

The following pages will present a method of downloading command data to the High Speed Counter card through the 32 consecutive input and output points that the module occupies in a Series 6 system. The data download routine is imbedded in a Demonstration program that uses a Series 6 with an Extended Instruction Set, 1024 registers, and an I/O Simulator Unit with a BCD display, 16 toggle switch inputs and 16 LED outputs.

With the Demonstration Program the user can enter commands into a command table. The command table is set-up within the Register Table of the CPU. The user

simply types the commands into the Register Table using a Program Development Terminal (PDT) or a WorkMaster. The program will step through the Register Table transferring the commands one by one from the table to the HSC.

In the Series Six system the I/O simulator uses input and output addresses 1 through 32. The High Speed Counter card is addressed at I/O points 33 through 64. Table 7 lists all of the Inputs, Outputs and Register address references that are used in the Demonstration Program.

OPERATION

The Demonstration Program is divided into two sections: the Main Body and a Subroutine. The Main Body contains the logic that performs the power up sequence required to enable the counter. The Subroutine does the actual loading of the Command Data to the HSC module. Figures 14 and 15 illustrate the operation of the Main Body and the Subroutine, respectively, in block diagram form. The function of each logic block with the corresponding rung numbers is described below.

TABLE 7. INPUT/OUTPUT AND REGISTER ALLOCATION CHART

Reference	Description
01 to 16 33 to 64	I/O Simulator High Speed Counter Module
01 to 016 033 to 064	I/O Simulator High Speed Counter Module
0201	Clear Power Up Bit
0202	Initiate Register Download
0203	Register Download In Progress
0204	Register Download Complete
0205	Command Byte Equals Zero
0206 to 0230	Detects Zero Data Byte Commands
0231,0232	Detects End of Register Table
0233	Update Simulator LED Outputs
0234	Indicates CB = 0 For Single Command Load
R12toR14	Scratch Registers
R15, R16	Stores Counts Per Time Base
R17 to R20	Scratch Registers
R21	Stores Command Byte Data
R22	Scratch Register
R23	Storage For 3rd Data Byte
R24	Pointer For Commands In the Register Table
R25 to R64	Table of HSC Commands
R65	Command Byte For Single Command Load
R66, R67	Data Bytes For Single Command Load
R74, R75	Return Data Bytes

MAIN BODY OF PROGRAM

(Refer to Figure 14)

Clear Power Up: Bit	This block sends CB = 6 to the HSC. The counter will only accept Command 1 (Reset Module) and Command 6 (Clear Power Up Bit) while the Power Up Bit is set. Rung Numbers: 24,25
Load Discrete: Set Up Data	The HSC outputs (in the default state) after power up are disabled. Also after power up the counter is disabled; meaning the HSC will ignore any incoming pulses. Here the Command Byte is set to zero (Discrete Commands) to enable the outputs and the counter. Rung Numbers: 2 - 7
Initiate: Register Load	This block contains the logic that initializes the register pointer to rest at the first register in the Register Table. Also a latch is set up that controls the operation of the Subroutine. While Command Data is being downloaded the latch is energized; if the last register in the table has been loaded the latch de-energizes, which terminates Subroutine execution. Rung Numbers: 24,26, 28
Last Register: Loaded	Here a check is performed to determine if the last register in the table has been loaded. As long as the register pointer has not reached the end of the table commands are downloaded to the HSC. Rung Numbers: 27
HSC Count/Outputs: Enabled and Download Complete	If the above check is true all commands in the table have been downloaded and the counter module will be enabled. Rung Numbers: 28
Execute: Subroutine	The Subroutine is executed one time to download a single command from Register Table to the High Speed card. Rung Numbers: 29,43 - 80

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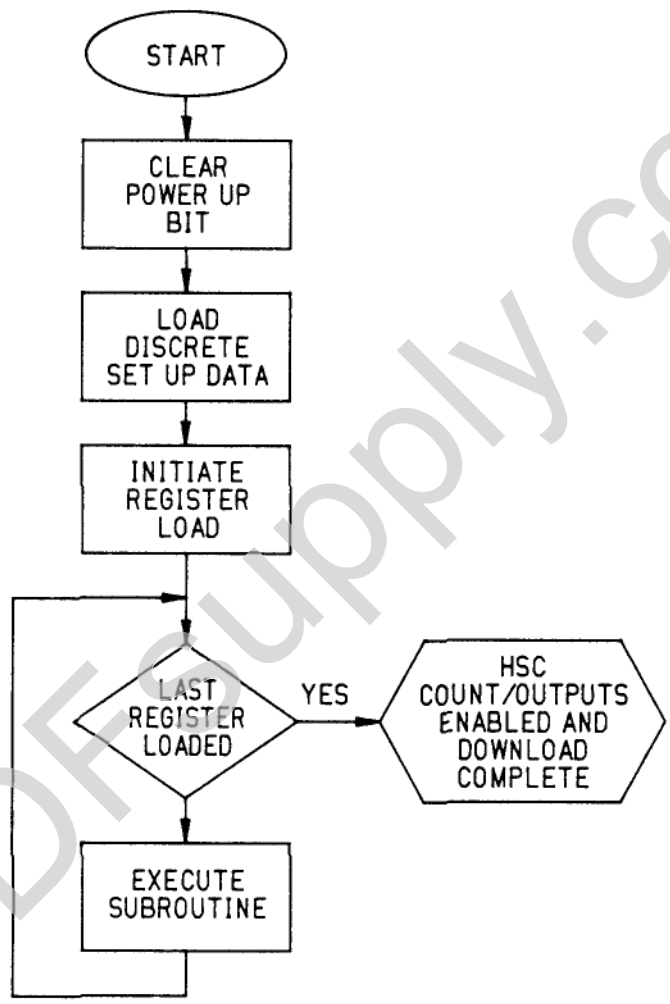


Figure 14. MAIN BODY OF PROGRAM

SUBROUTINE

(Refer to Figure 151)

Read Command:	Read the Command Byte from the register in the Register Table upon which the register pointer resides. Store the Command Byte in a buffer register. (Increment the pointer.) Rung Numbers: 44
Last Register:	This block performs a check to determine if the previously read command resides in the last register in the Register Table. Rung Numbers: 44
'0' D.B.: Command Detected	Here a check is performed to determine whether or not the command requires Data Bytes. Rung Numbers: 45 - 68
'0' Register: Value	If the command does not require any Data Bytes, check the Command Byte for a value of zero (Discrete Commands or no commands). Rung Numbers: 69, 70
Clear 1st and: 2nd D.B.	If a zero Data Byte Command is detected clear the data byte buffer registers. Rung Numbers: 70
Clear 3rd D.B.	
Read 1st and: 2nd D.B.	If the command requires data read the 1st and 2nd Data Bytes from the Register Table and store them in a buffer register. (Increment pointer.) Rung Numbers: 71
Read 3rd D.B.:	Read the 3rd Data Byte and store it in a buffer register. (Increment Pointer.) Rung Numbers: 72
Load Command: Byte	Load the Command Byte from the storage register to the Output Table. Rung Numbers: 73
Load 1st and: 2nd D.B.	Move the 1st and 2nd Data Bytes from the buffer storage register to the Output Table. Rung Numbers: 73
Load 3rd D.B.:	Move the 3rd Data Byte from its buffer register to the Output Table. Rung Numbers: 73

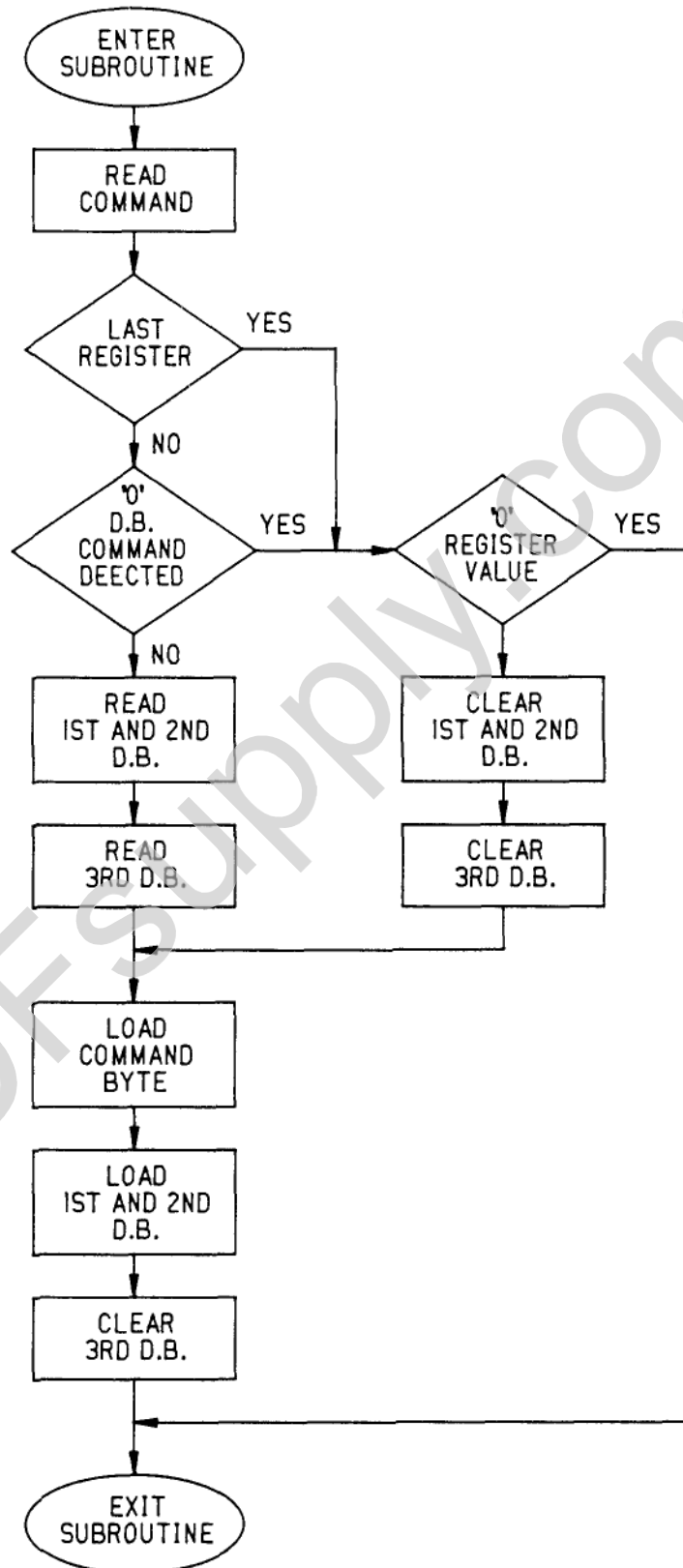


Figure 15. SUBROUTINE

ENTERING COMMAND DATA

The High Speed Counter commands are entered into a table that consists of a block of registers located in the CPU Register Table. In the Demonstration Program the first register in the table is R25 and the last register is R64. Each command will occupy either one or three registers depending upon the command. Commands that require no Data Bytes use one register: commands that require data use 3 registers.

For the Command Byte, the command number is entered as a single precision decimal number into the Register Table. The Data Bytes, if required, are entered as a double precision number into the next two registers in the table. The Figure 17 below illustrates how the commands would appear in the Register Table on a PDT.

TABLE 8. CPU REGISTER TABLE

REGISTER 0025									
0024	0000	0000	0000	0000	0000	0000	0000	0000	0017
0032	0000	0000	0000	0000	0000	0000	0000	0000	0025
0040	0000	0000	0000	0000	0000	0000	0000	0000	0033
0048	0000	0000	0000	0000	0000	0000	0000	0000	0042

The above illustration shows four commands. Command 33 (Load Upper Count Limit) resides in R25. Located in R26 and R27 are the Data Bytes (+ 9999) associated with CB = 33. R28 contains the command to "Load the Lower Count Limit" of the HSC (CB - 34). The data for this command is located in R29 and R30 (-9999). R33 contains a value of 64. CB = 64 (Return Accumulate Register) does not require any Data Bytes, so the next command in the table is located in R34.

I/O SIMULATOR

The I/O Simulator is used to activate the inputs that download the data to the HSC, latch the HSC outputs, load a single command and reset the counter module. The Series 6 CPU uses outputs on the simulator to display the count or error codes, and provide diagnostic information with the LED indicator lights. Figure 16 and Tables 7 and 8 give the simulator I/O functions.

NOTE

Command 64 could also have been entered into R31, and CB = 36 could have been placed in R32. If Command 36 had been placed in R32 the Data Bytes would be entered into R33 and R34.

The BCD display will display the accumulate count value of the High Speed Counter by default. If the HSC module generates an error code, the error code will be displayed.

TABLE 9. SIMULATOR INPUTS

Toggle Switch #	Function
11	Reset the High Speed Counter Module. Send CB = 1.
12	Clear the Power Up Bit and Download the Command Table to the HSC.
13	Abort the Home Search, Send CB - 5.
14	Reset the Accumulate Count Register to its Lower Limit.
15 through 18	Latch/Unlatch HSC outputs 1 through 4.
19	Return Preset Comparison States.
110	Return the Counts per Time Base and Store the number of counts in R15 and 16.
111	Load the single command located in R65, R66, and R67. (R65 contains the Command Byte and R66 and R67 contains the Data Bytes.

SIMULATOR OUTPUTS

TABLE 10 SIMULATOR OUTPUTS

LED Light #	Function
01	Counting is Enabled
02	The Power Up Bit has been cleared and the commands have been downloaded.
03	Energized when the external power supply is out of tolerance.
04	Turns on when an error condition exists.
05 through 08	Indicates the HSC Preset Comparison States when switch 19 is "on".
08	Energized when number on BCD display is negative.
113 through 016	Reflects the HSC Outputs Preset Comparison Senses as determined by CB = 35.
017 through 032	Simulator LED Display.

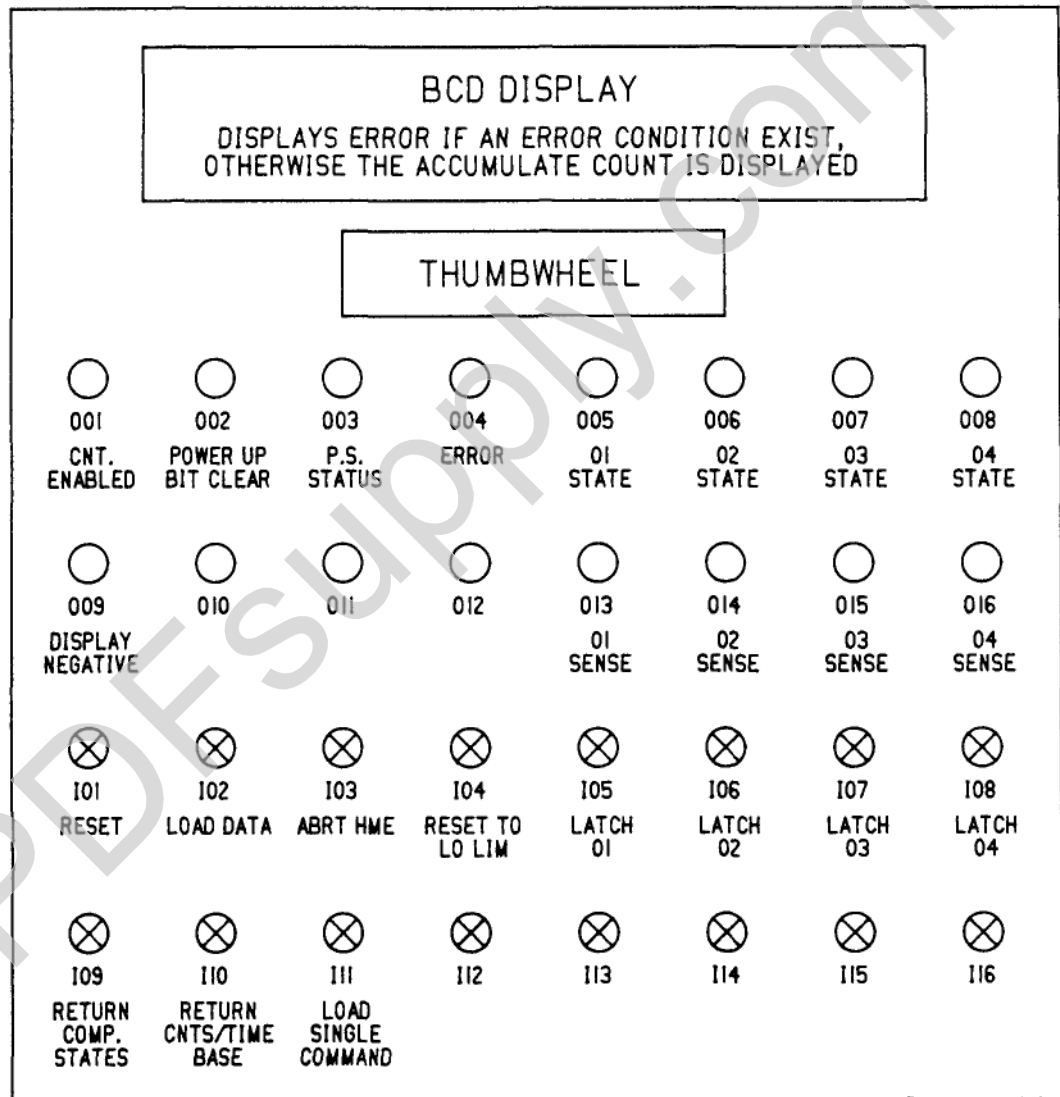


Figure 16. I/O SIMULATOR

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 REGISTER TABLE METHOD

```

GGGGGG      EEEEEEEE
GGGGGGGG    EEEEEEEE
GG           EE
GG          EE
GG  GGGGG   EEEEEEE
GG      GG  EE
GG      GG  EE
GGGGGGGG    EEEEEEEE
GGGGGG      EEEEEEEE
  
```

```

SSSSSS      EEEEEEEE      RRRRRR      II      EEEEEEEE      SSSSSS
SSSSSSSS    EEEEEEEE    RRRRRRRR    II      EEEEEEEE    SSSSSSSS
SS          EE          RR      RR      II      EE          SS
SS          EE          RR      RR      II      EE          SS
  SSSSSS    EEEEEEE    RRRRRR      II      EEEEEEE    SSSSSS
          SS          EE          RR      RR      II      EE          SS
          SS          EE          RR      RR      II      EE          SS
SSSSSSSS    EEEEEEEE    RR      RR      II      EEEEEEEE    SSSSSSSS
SSSSSS      EEEEEEEE    RR      RR      II      EEEEEEEE    SSSSSS
  
```

```

SSSSSS      II      XX      XX
SSSSSSSS    II      XX      XX
SS          II      XX      XX
SS          II      XX      XX
  SSSSSS    II      XXX
          SS      II      XX      XX
          SS      II      XX      XX
SSSSSSSS    II      XX      XX
SSSSSS      II      XX      XX
  
```

```

*****
*
*      INSTRUCTION SET: EXTENDED
*      CPU ID: 2
*      CPU MEMORY SIZE: 4096
*      PROGRAM MEMORY SIZE: 434
*      REGISTER MEMORY SIZE: 1024
*
*****
  
```

GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

: << RUNG      0 >>
:
: *****
: *
: *   The logic in this Demonstration Program is divided and
: *   prioritized to avoid the interlocking that would have
: *   been necessary otherwise. In the program the Reset
: *   Command (CB = 1), activated by I1, is given the highest
: *   priority and the single command load, activated by I11,
: *   is given the lowest priority.
: *
: *
: *****
:
+ [ Start of Program ]-
:
: << RUNG      1 >>
:
+ [ NO OP ]-
:
: << RUNG      2 >>
:
: *****
: *
: *   The program is initially set up to send the Discrete Command
: *   set to the High Speed Counter Module. (If the outputs associated
: *   with the HSC are not cleared the last command downloaded will be
: *   sent to the module repeatedly.) Also this allows specific commands
: *   to be activated by the toggle switch inputs on the I/O Simulator.
: *
: *
: *   033      CmdByte      HSC Command Byte
: *   049      DatByte2     HSC 2nd Data Byte
: *
: *****
:
:          CmdByte          DatByte2
: Const    00033      Const    00049
+ [ A      MOVE      B ]- [ A      MOVE      B ]-
!+00000          +00000
:
  
```


GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

<< RUNG  11 >>
Rt_C/TB 1stRtDB           C/TB_12 3rdRtDB           C/TB_3
I0010  I0041           R0015  I0057           R0016
+---] [---] [ A      MOVE      B ]-[ MOVE RIGHT 8 BITS ]-      ( )

<< RUNG  12 >>
*****
*
*   Input 9 uses the "Return Comparison States" to allow the S6
*   CPU to energize outputs (Simulator LED Outputs 5 to 8).
*
*   19      Rt_CpSt      Return Preset Comparison States
*   149     2ndRtDB      HSC 2nd Return Data Byte
*   150     Rtrn_18      HSC Return Data_Input Bit 18
*   151     Rtrn_19      HSC Return Data_Input Bit 19
*   152     Rtrn_20      HSC Return Data_Input Bit 20
*   05      01CmpSt      HSC Output 1 Preset Comparison State
*   06      02CmpSt      HSC Output 2 Preset Comparison State
*   07      03CmpSt      HSC Output 3 Preset Comparison State
*   08      04CmpSt      HSC Output 4 Preset Comparison State
*   053     Dact_21      Discrete Data_HSC Output Bit 21
*
*****
Rt_CpSt                                Dact_21
I0009                                    00053
+---] [-----] [-----] [-----] [-----] [-----] [-----] ( )

<< RUNG  13 >>
Rt_CpSt 2__RtDB           01CmpSt
I0009  I0049           00005
+---] [-----] [-----] [-----] [-----] [-----] [-----] [LATCH]--- ( L )
( )
Rt_CpSt 2__RtDB           ( )
I0009  I0049           ( )
+---] [-----] [-----] [-----] [-----] [-----] [-----] (UL)

<< RUNG  14 >>
Rt_CpSt Rtrn_18           02CmpSt
I0009  I0050           00006
+---] [-----] [-----] [-----] [-----] [-----] [-----] [LATCH]--- ( L )
( )
Rt_CpSt Rtrn_18           ( )
I0009  I0050           ( )
+---] [-----] [-----] [-----] [-----] [-----] [-----] (UL)

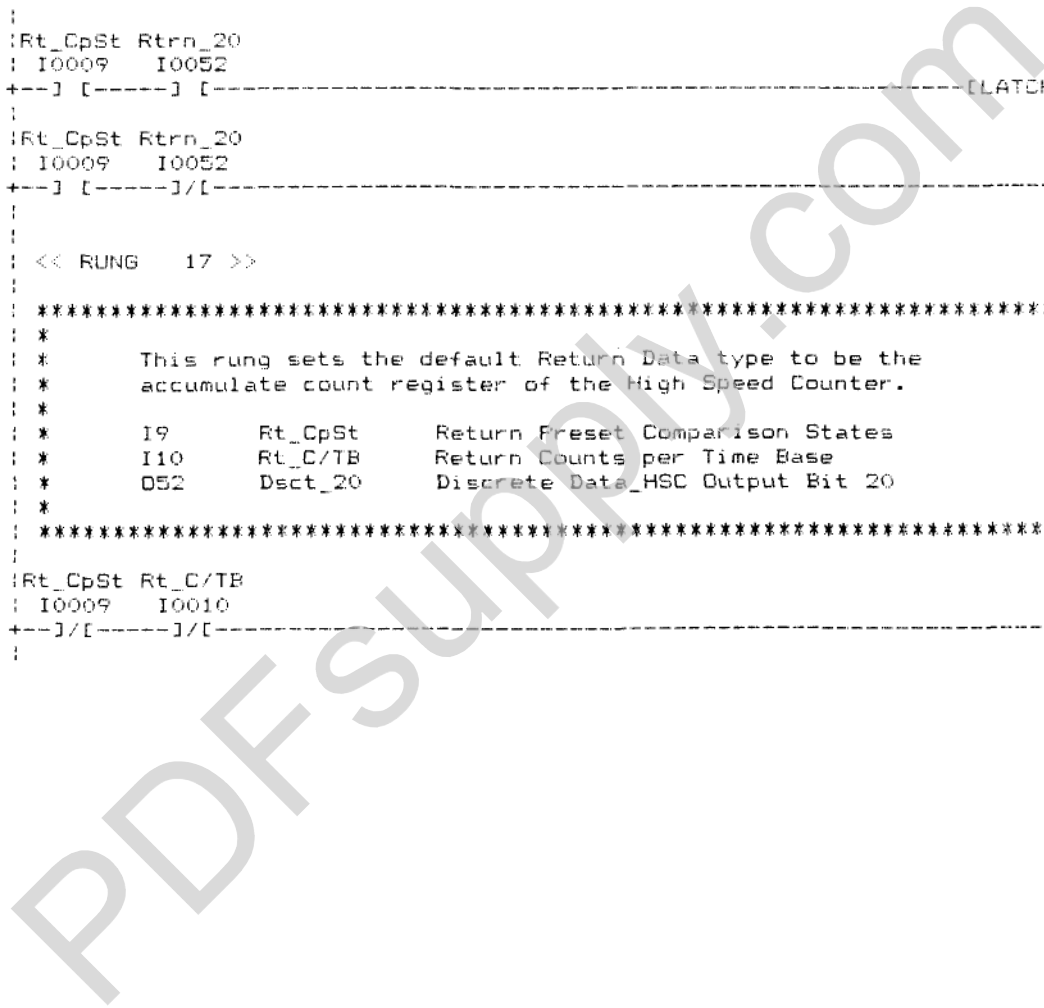
```

GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

|
| << RUNG 15 >>
|
| Rt_CpSt Rtrn_19                                03CmpSt
| I0009 I0051                                00007
|-----] [-----] [-----] [-----] [LATCH]---- ( L )
|
| Rt_CpSt Rtrn_19                                ( )
| I0009 I0051                                ( )
|-----] [-----] / [-----] / [-----] (UL)
|
| << RUNG 16 >>
|
| Rt_CpSt Rtrn_20                                04CmpSt
| I0009 I0052                                00008
|-----] [-----] [-----] [-----] [LATCH]---- ( L )
|
| Rt_CpSt Rtrn_20                                ( )
| I0009 I0052                                ( )
|-----] [-----] / [-----] / [-----] (UL)
|
| << RUNG 17 >>
|
| *****
| *
| * This rung sets the default Return Data type to be the
| * accumulate count register of the High Speed Counter.
| *
| * 19 Rt_CpSt Return Preset Comparison States
| * I10 Rt_C/TB Return Counts per Time Base
| * 052 Dsct_20 Discrete Data_HSC Output Bit 20
| *
| *****
|
| Rt_CpSt Rt_C/TB                                Dsct_20
| I0009 I0010                                00052
|-----] / [-----] / [-----] ( )
|

```



GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

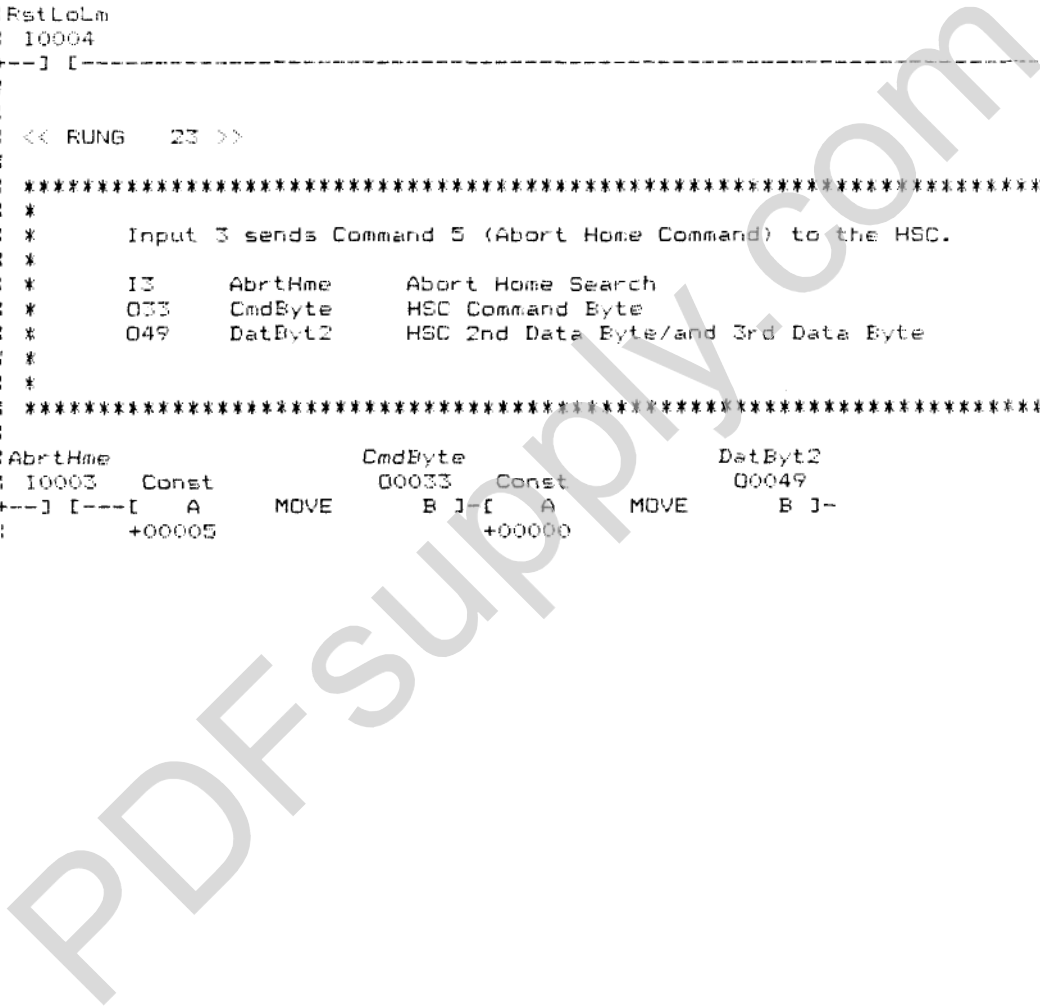
: << RUNG 18 >>
:
: *****
: *
: * Inputs 8,7,6, and 5 utilize the Discrete Commands to latch
: * and unlatch the Preset Comparison States of the four HSC
: * Outputs.
: *
: * I5 Latch_1 Latch HSC Output 1
: * I6 Latch_2 Latch HSC Output 2
: * I7 Latch_3 Latch HSC Output 3
: * I8 Latch_4 Latch HSC Output 4
: * O47 Dsct_15 Discrete Data__HSC Output Bit 15
: * O48 Dsct_16 Discrete Data__HSC Output Bit 16
: * O49 Dsct_17 Discrete Data__HSC Output Bit 17
: * O50 Dsct_18 Discrete Data__HSC Output Bit 18
: *
: *****
: Latch_4 Dsct_18
: I000B 00050
: ] [----- ( )
:
: << RUNG 19 >>
: Latch_3 DatByt2
: I0007 00049
: ] [----- ( )
:
: << RUNG 20 >>
: Latch_2 Dsct_16
: I0006 00048
: ] [----- ( )
:
: << RUNG 21 >>
: Latch_1 Dsct_15
: I0005 00047
: ] [----- ( )
:

```

GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

: << RUNG 22 >>
: *****
: *
: *      Input 4 will reset the accumulate count register in the HSC
: *      to its lower limit.
: *
: *      I4      RstLoLm      Rst Accumulate Register To Lower Limit
: *      051     Dscnt_19     Discrete Data__HSC Output Bit 19
: *
: *****
: RstLoLm                                     Dscnt_19
: 10004                                         00051
:-----] [-----]-----] [-----]-----] [-----] ( )
:
: << RUNG 23 >>
: *****
: *
: *      Input 3 sends Command 5 (Abort Home Command) to the HSC.
: *
: *      I3      AbrtHme      Abort Home Search
: *      033     CmdByte      HSC Command Byte
: *      049     DatByt2      HSC 2nd Data Byte/and 3rd Data Byte
: *
: *****
: AbrtHme      CmdByte      DatByt2
: 10003  Const  00033  Const  00049
:-----] [---] [---] [---] [---] [---] [---] [---] [---] [---] [---] ( )
:      +00005      +00000
  
```



GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

<< RUNG 24 >>

```

*****
*
*   When Input 2 is on it performs multiple functions. In the
*   1st Scan after the input is actived Command 6 is issued to
*   clear the Power-Up Bit. In the 2nd Scan the Subroutine is
*   activated which downloads the commands stored in the
*   Register Table.
*
*   I2      Ld_Cnds      Clear Power Up Bit/Download Data to HSC
*   003     CmdByte     HSC Command Byte
*   0201    ClPwrBt     One Shot To Clear Power Up Bit
*   0202    InitDld     One Shot To Initiate Register Download
*
*****

```

```

Ld_Cnds                                ClPwrBt
I0002                                  00201
+---] [-----] (OS)

```

<< RUNG 25 >>

```

ClPwrBt                                CmdByte
00201  Const                          00033
+---] [---] [ A      MOVE      B ]-      ( )
      +00006

```

<< RUNG 26 >>

```

ClPwrBt                                InitDld
00201                                  00202
+---] [-----] (OS)

```

GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

:
: << RUNG 27 >>
:
: *****
: *
: * 0232 and 0231 are flags that are turned on when the last
: * register in the Register Table has been downloaded to the
: * HSC. When 0232 and 0231 are on the Subroutine ceases operation.
: *
: * 0202 InitDld One Shot To Initiate Register Download
: * 0203 Dld_On Register Download In Progress
: * 0204 Dld_Off Register Table Download Complete
: * 0231 EOTble1 Flag 1_End Of Register Table
: * 0232 EOTble2 Flag 2_End Of Register Table
: * R14 Srtch_3 Scratch Register
: * R24 Reg_Ptr Pointer For Register Table
: *
: *****
: EOTble2 Dld_Off
: 00232 00204
: +---] [-----] (OS)
:
: EOTble1
: 00231
: +---] [-----]
:
: << RUNG 28 >>
:
: InitDld Reg_Ptr Dld_On
: 00202 Const R0024 00203
: +---] [---] [ A MOVE B ]-----] [LATCH]---] ( L )
: | +00000
: | Dld_Off ( )
: | 00204 ( )
: +---] [-----] (UL)
:
: << RUNG 29 >>
:
: Dld_On Srtch_3 Srtch_3
: 00203 Const R0014 Const R0014
: +---] [---] [ A MOVE B ]-[ DO SUB N REPS ]- ( )
: | +00001 001
  
```

GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

  << RUNG   30 >>
  *****
  *
  *      Toggle Switch Input 1 resets the Preset Registers, the
  *      Discrete Commands, and the HSC Outputs. (The Power-Up
  *      Bit is also set when Command 1 is sent.)
  *
  *      I1      Reset      Reset the High Speed Counter Module
  *      O33     CmdByte    HSC Command Byte
  *
  *
  *****
  Reset                               CmdByte
  I0001  Const                        00033
  +---] [---] [ A      MOVE      B ]- ( )
          +00001

  << RUNG   31 >>

+ [NO OP]- ( )

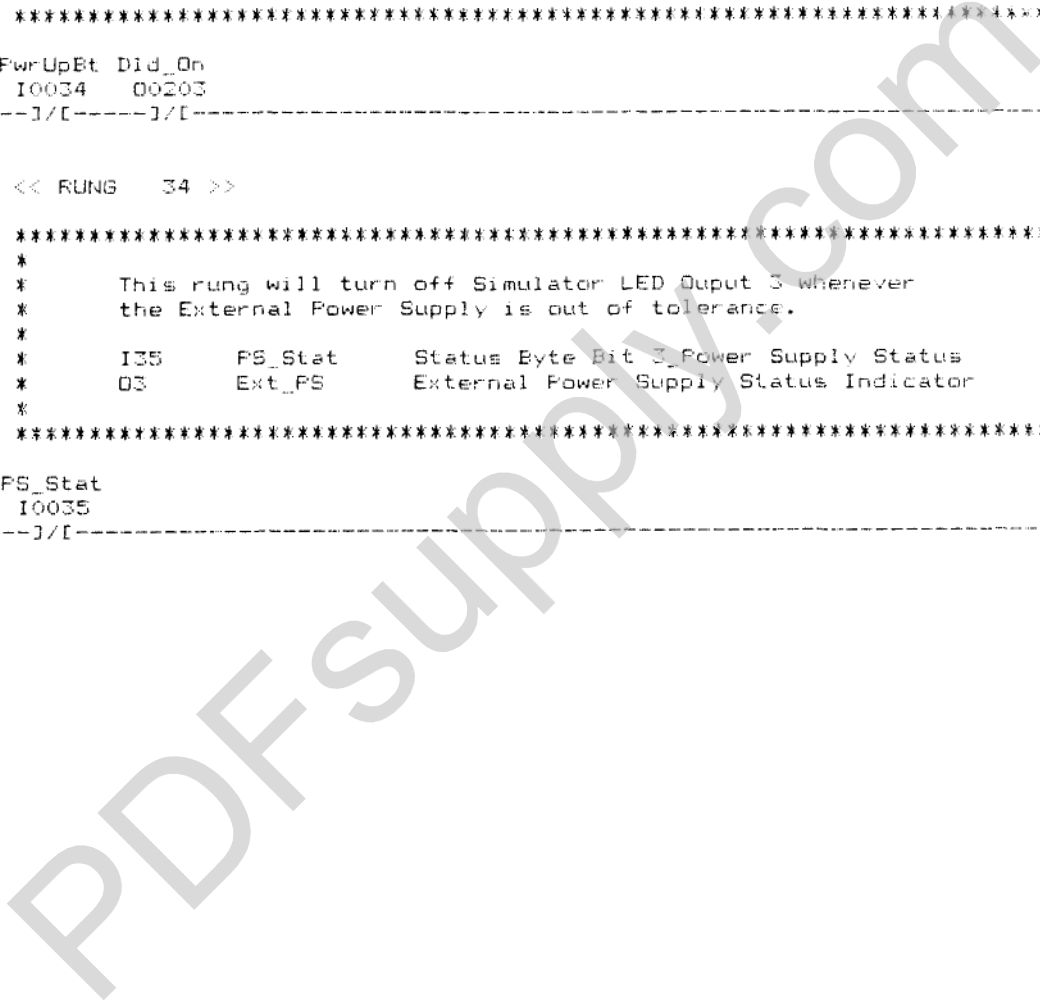
  << RUNG   32 >>
  *****
  *
  *      Input 36 (Status Byte Bit 4) energizes O1 (Simulator LED
  *      Output 1) whenever the HSC count is enabled.
  *
  *      I36     EnblBit     Status Byte Bit 4
  *      O1      CntEnbl     Counting Is Enabled
  *
  *
  *****
  EnblBit                               CntEnbl
  I0036                                 00001
  +---] [-----] ( )
  
```


GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

  << RUNG 33 >>
  *****
  *
  *   After the Register Table is downloaded to the HSC and
  *   the Power-Up Bit has been cleared Simulator LED Output 2
  *   is energized.
  *
  *   I34      FwrUpBt      Status Byte Bit 2_Power Up Bit
  *   02      DldCmpt      Power Up Bit Clear & Download Complete
  *   0203    Dld_On       Register Download Complete
  *
  *****
  FwrUpBt Dld_On                                     DldCmpt
  I0034   00203                                     00002
  +---] / [-----] / [-----] ( )

  << RUNG 34 >>
  *****
  *
  *   This rung will turn off Simulator LED Output 3 whenever
  *   the External Power Supply is out of tolerance.
  *
  *   I35      PS_Stat      Status Byte Bit 3_Power Supply Status
  *   03      Ext_PS       External Power Supply Status Indicator
  *
  *****
  PS_Stat                                     Ext_PS
  I0035                                     00003
  +---] / [-----] / [-----] ( )
  
```



GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

:
: << RUNG 35 >>
:
: *****
: *
: * When the "Return Data Type" input points indicate an error
: * condition Simulator LED Output 4 turns on and the Simulator
: * displays the error code.
: *
: * I38 DatTyp1 Status Byte Bit 6_Return Data Type
: * I39 DatTyp2 Status Byte Bit 7_Return Data Type
: * I40 DatTyp3 Status Byte Bit 8_Return Data Type
: * I41 1stRtDB HSC 1st Return Data Byte
: * 04 Error Error Condition Exists
: * 017 SimDply Simulator BCD Display
: * R74 RtDta12 1st & 2nd Data Bytes HSC Return Data
: *
: *****
:
: DatTyp1 DatTyp2 DatTyp3 Const RtDta12 Error
: I0038 I0039 I0040 Const R0074 00004
+---] / [-----] / [-----] [---[ A MOVE B ]----- ( )
: +00000
:
: << RUNG 36 >>
:
: DatTyp1 DatTyp2 DatTyp3 1stRtDB RtDta12 RtDta12 SimDply
: I0038 I0039 I0040 I0041 R0074 R0074 00017
+---] / [-----] / [-----] [---[ MOVE RIGHT 8 BITS ]-[ BIN TO BCD ]- ( )
:
: << RUNG 37 >>
:
: *****
: *
: * This rung will energize Simulator LED Duput 9 whenever
: * a negative accumulate count value is returned to the S6
: * CPU.
: *
: * I64 NumSign HSC Return Data_Input Bit 32/Sign Bit
: * 09 Neg_Num Number on Simulator Display is Negative
: * R17 Srtch_4 Scratch Register
: *
: *****
:
: NumSign Const Srtch_4 Srtch_4 Srtch_4 Const Neg_Num
: I0064 Const R0017 R0017 R0017 Const 00009
+---] [---[ A MOVE B ]-[ A INV B LEN ]----- ( )
: +00000 001
  
```

GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

  << RUNG   38 >>
  *****
  *
  *   After the "Invert" Instruction is executed on R17 this
  *   rung performs a sign extension on R75 to convert the 3 bytes
  *   of HSC Return Data into 4 bytes of 56 Double Precision Data
  *   (R74 and R75). The value in R74 is then converted to a positive
  *   4 digit BCD number to be displayed on the I/O Simulator.
  *
  *   I38      DatTyp1      Status Byte Bit 6_Return Data Type
  *   I39      DatTyp2      Status Byte Bit 7_Return Data Type
  *   I40      DatTyp3      Status Byte Bit 8_Return Data Type
  *   I41      1stRtDB      HSC 1st Return Data Byte
  *   I64      NumSign      HSC Return Data_Input Bit 32/Sign Bit
  *   O17      SimDply      Simulator BCD Display
  *   R17      Srtch_4      Scratch Register
  *   R18      Srtch_5      Scratch Register
  *   R74      RtDta12      1st & 2nd Data Bytes HSC Return Data
  *   R75      RtDta3      3rd Data Byte HSC Return Data
  *
  *****
  1stRtDB RtDta12 3rdRtDB      RtDta3 NumSign Srtch_4      RtDta3
  : I0041 R0074 I0057      R0075 I0064 R0017      R0075
+ [ I/O 10 REG ]-[ A MOVE B ]-[ ]-[ MOVE LEFT 8 BITS ]- ( )
  :
  << RUNG   39 >>
  NumSign      1stRtDB Srtch_5
  : I0064 Const I0041 R0018
+ --] [---[ A SUBX B = C ]- ( )
  : +00000
  :
  << RUNG   40 >>
  NumSign 1stRtDB      Srtch_5
  : I0064 I0041 R0018
+ --] / [---[ A MOVE B ]- ( )
  :
  << RUNG   41 >>
  DatTyp1 DatTyp2 DatTyp3 Srtch_5 SimDply
  : I0038 I0039 I0040 R0018 O0017
+ --] / [---] / [---] / [---[ BIN TO BCD ]- ( )
  :
  << RUNG   42 >>
  :
+ [NO OP]- ( )
  :
  
```


GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

  << RUNG   45 >>
  *****
  *
  *   The next 26 rungs of logic check for commands that do not
  *   require any Data Bytes.
  *
  *   0205      0_Dtcd      Zero Value In Register Detected
  *   0206      Cm01Dtd     Command 1 Detected
  *   0207      Cm02Dtd     Command 2 Detected
  *   0208      Cm04Dtd     Command 4 Detected
  *   0209      Cm05Dtd     Command 5 Detected
  *   0210      Cm06Dtd     Command 6 Detected
  *   0211      Cm48Dtd     Command 48 Detected
  *   0212      Cm49Dtd     Command 49 Detected
  *   0213      Cm50Dtd     Command 50 Detected
  *   0214      Cm51Dtd     Command 51 Detected
  *   0215      Cm52Dtd     Command 52 Detected
  *   0216      Cm53Dtd     Command 53 Detected
  *   0217      Cm54Dtd     Command 54 Detected
  *   0218      Cm55Dtd     Command 55 Detected
  *   0219      Cm56Dtd     Command 56 Detected
  *   0220      Cm57Dtd     Command 57 Detected
  *   0221      Cm58Dtd     Command 58 Detected
  *   0222      Cm59Dtd     Command 59 Detected
  *   0223      Cm64Dtd     Command 64 Detected
  *   0224      Cm65Dtd     Command 65 Detected
  *   0225      Cm66Dtd     Command 66 Detected
  *   0226      Cm67Dtd     Command 67 Detected
  *   0227      Cm68Dtd     Command 68 Detected
  *   R21       Stor_CB     Storage For Command Byte
  *   R22       Srtch_7     Scratch Register
  *
  *****
  |
  |           Srtch_7 Srtch_7 Stor_CB
  | Const      R0022  R0022  R0021
  |[ A      MOVE      B ]-[ A :   B ]----- ( )
  |+00000
  |
  | << RUNG   46 >>
  |
  |           Srtch_7 Srtch_7 Stor_CB
  | Const      R0022  R0022  R0021
  |[ A      MOVE      B ]-[ A :   B ]----- ( )
  |+00001
  |
  | << RUNG   47 >>
  |
  |           Srtch_7 Srtch_7 Stor_CB
  | Const      R0022  R0022  R0021
  |[ A      MOVE      B ]-[ A :   B ]----- ( )
  |+00002
  
```

GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

  << RUNG  48 >>
  Const          Srtch_7 Srtch_7 Stor_CB          Cm04Dtd
                 R0022  R0022  R0021          00208
+ [  A          MOVE          B ]-[  A :    B ]----- ( )
|+00004
  << RUNG  49 >>
  Const          Srtch_7 Srtch_7 Stor_CB          Cm05Dtd
                 R0022  R0022  R0021          00209
+ [  A          MOVE          B ]-[  A :    B ]----- ( )
|+00005
  << RUNG  50 >>
  Const          Srtch_7 Srtch_7 Stor_CB          Cm06Dtd
                 R0022  R0022  R0021          00210
+ [  A          MOVE          B ]-[  A :    B ]----- ( )
|+00006
  << RUNG  51 >>
  Const          Srtch_7 Srtch_7 Stor_CB          Cm48Dtd
                 R0022  R0022  R0021          00211
+ [  A          MOVE          B ]-[  A :    B ]----- ( )
|+00048
  << RUNG  52 >>
  Const          Srtch_7 Srtch_7 Stor_CB          Cm49Dtd
                 R0022  R0022  R0021          00212
+ [  A          MOVE          B ]-[  A :    B ]----- ( )
|+00049
  << RUNG  53 >>
  Const          Srtch_7 Srtch_7 Stor_CB          Cm50Dtd
                 R0022  R0022  R0021          00213
+ [  A          MOVE          B ]-[  A :    B ]----- ( )
|+00050
  << RUNG  54 >>
  Const          Srtch_7 Srtch_7 Stor_CB          Cm51Dtd
                 R0022  R0022  R0021          00214
+ [  A          MOVE          B ]-[  A :    B ]----- ( )
|+00051
  << RUNG  55 >>
  Const          Srtch_7 Srtch_7 Stor_CB          Cm52Dtd
                 R0022  R0022  R0021          00215
+ [  A          MOVE          B ]-[  A :    B ]----- ( )
|+00052
  
```

GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

  << RUNG   56 >>
  Const          Srtch_7 Srtch_7 Stor_CB          Cm53Dtd
                  R0022  R0022  R0021          00216
+ [ A MOVE      B ]-[ A : B ]----- ( )
!+00053

  << RUNG   57 >>
  Const          Srtch_7 Srtch_7 Stor_CB          Cm54Dtd
                  R0022  R0022  R0021          00217
+ [ A MOVE      B ]-[ A : B ]----- ( )
!+00054

  << RUNG   58 >>
  Const          Srtch_7 Srtch_7 Stor_CB          Cm55Dtd
                  R0022  R0022  R0021          00218
+ [ A MOVE      B ]-[ A : B ]----- ( )
!+00055

  << RUNG   59 >>
  Const          Srtch_7 Srtch_7 Stor_CB          Cm56Dtd
                  R0022  R0022  R0021          00219
+ [ A MOVE      B ]-[ A : B ]----- ( )
!+00056

  << RUNG   60 >>
  Const          Srtch_7 Srtch_7 Stor_CB          Cm57Dtd
                  R0022  R0022  R0021          00220
+ [ A MOVE      B ]-[ A : B ]----- ( )
!+00057

  << RUNG   61 >>
  Const          Srtch_7 Srtch_7 Stor_CB          Cm58Dtd
                  R0022  R0022  R0021          00221
+ [ A MOVE      B ]-[ A : B ]----- ( )
!+00058

  << RUNG   62 >>
  Const          Srtch_7 Srtch_7 Stor_CB          Cm59Dtd
                  R0022  R0022  R0021          00222
+ [ A MOVE      B ]-[ A : B ]----- ( )
!+00059

  << RUNG   63 >>
  Const          Srtch_7 Srtch_7 Stor_CB          Cm64Dtd
                  R0022  R0022  R0021          00223
+ [ A MOVE      B ]-[ A : B ]----- ( )
!+00064
  
```

GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

:
: << RUNG 64 >>
:
:           Srtch_7 Srtch_7 Stor_CB           Cm65Dtd
: Const    R0022  R0022  R0021           00224
+[ A      MOVE    B ]-[ A : B ]----- ( )
: +00065
:
: << RUNG 65 >>
:
:           Srtch_7 Srtch_7 Stor_CB           Cm66Dtd
: Const    R0022  R0022  R0021           00225
+[ A      MOVE    B ]-[ A : B ]----- ( )
: +00066
:
: << RUNG 66 >>
:
:           Srtch_7 Srtch_7 Stor_CB           Cm67Dtd
: Const    R0022  R0022  R0021           00226
+[ A      MOVE    B ]-[ A : B ]----- ( )
: +00067
:
: << RUNG 67 >>
:
:           Srtch_7 Srtch_7 Stor_CB           Cm68Dtd
: Const    R0022  R0022  R0021           00227
+[ A      MOVE    B ]-[ A : B ]----- ( )
: +00068

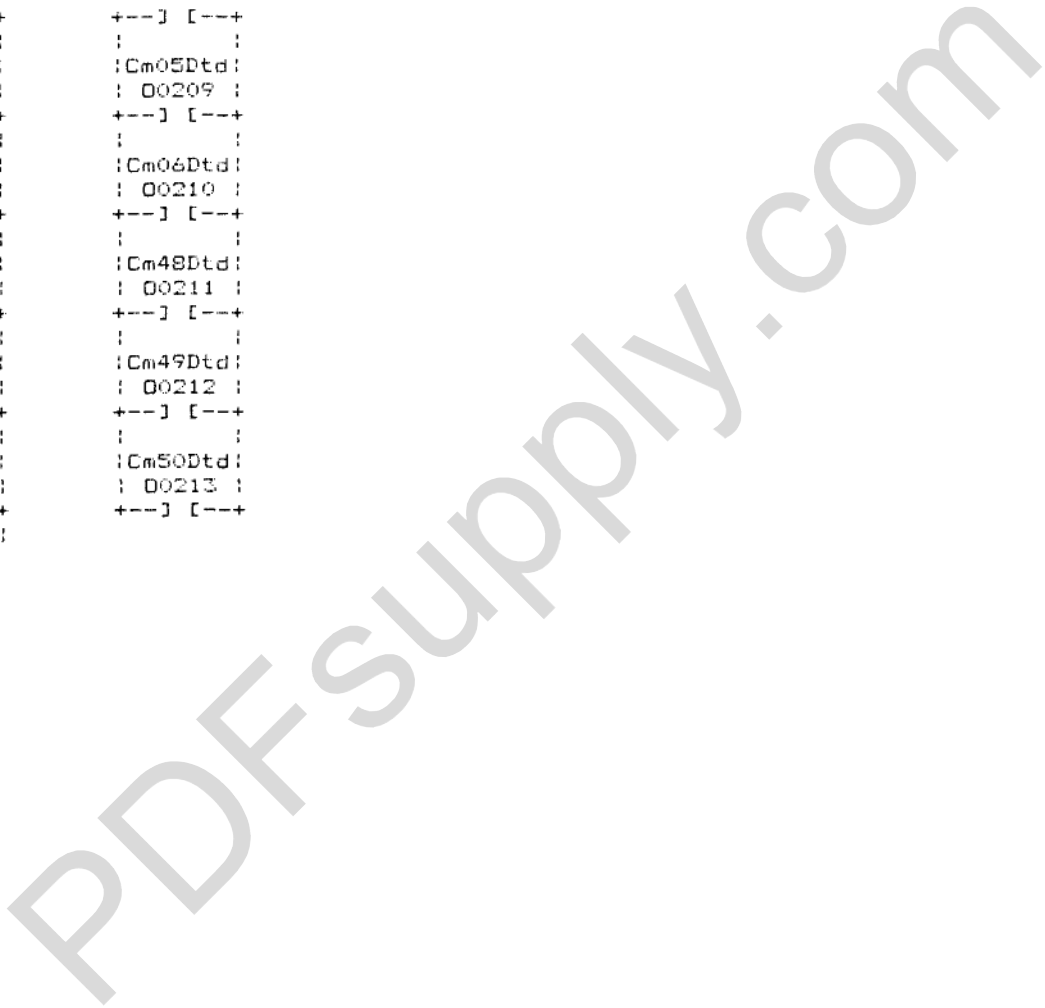
```


GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

:
: << RUNG 68 >>
:
: O_Dtd  Cm01Dtd  O_Dtd1
: 00205  00206  00228
:-----] / [-----] [-----] ( )
:
: | Cm02Dtd |
: | 00207 |
+ | +---] [---+
: |
: | Cm04Dtd |
: | 00208 |
+ | +---] [---+
: |
: | Cm05Dtd |
: | 00209 |
+ | +---] [---+
: |
: | Cm06Dtd |
: | 00210 |
+ | +---] [---+
: |
: | Cm48Dtd |
: | 00211 |
+ | +---] [---+
: |
: | Cm49Dtd |
: | 00212 |
+ | +---] [---+
: |
: | Cm50Dtd |
: | 00213 |
+ | +---] [---+
:
:

```



GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

:
: << RUNG 69 >>
:
: O_Dtcd Cm51Dtd O_Dtcd2
: 00205 00214 00229
+---] / [---] [---] [---] ( )
:
: Cm52Dtd:
: 00215 :
+---] [---]
:
: Cm53Dtd:
: 00216 :
+---] [---]
:
: Cm54Dtd:
: 00217 :
+---] [---]
:
: Cm55Dtd:
: 00218 :
+---] [---]
:
: Cm56Dtd:
: 00219 :
+---] [---]
:
: Cm57Dtd:
: 00220 :
+---] [---]
:
: Cm58Dtd:
: 00221 :
+---] [---]
:
:

```

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GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

<< RUNG 70 >>

```

*****
*
*      IF a Zero Data Byte Command is detected the Data Byte
*      storage registers (R22and R23) are cleared.
*
*      0205      O_RqVal      Zero Value In Register Detected
*      0223      Cm64Dtd     Command 64 Detected
*      0224      Cm65Dtd     Command 65 Detected
*      0225      Cm66Dtd     Command 66 Detected
*      0226      Cm67Dtd     Command 67 Detected
*      0227      Cm68Dtd     Command 68 Detected
*      0228      O_Dtcd1     Flag 1_Zero Data Byte Detected
*      0229      O_Dtcd2     Flag 2_Zero Data Byte Detected
*      0230      O_Dtcd3     Flag 3_Zero Data Byte Detected
*      R22       Srtch_7     Scratch Register/1st and 2nd Data Bytes
*      R23       3rd_DB     Storage For 3rd Data Byte
*
*****

```

```

O_Dtcd  Cm59Dtd          Srtch_7          3rd_DB          O_Dtcd3
00205  00222  Const      R0022  Const      R0023          00230
+---] / [---+ ] [---+ [ A      MOVE      B ]-[ A      MOVE      B ]----- ( )
|
|      |      | +00000          +00000
|      | Cm64Dtd |
|      | 00223 |
+---+ +---] [---+
|      |      |
|      | Cm65Dtd |
|      | 00224 |
+---+ +---] [---+
|      |      |
|      | Cm66Dtd |
|      | 00225 |
+---+ +---] [---+
|      |      |
|      | Cm67Dtd |
|      | 00226 |
+---+ +---] [---+
|      |      |
|      | Cm68Dtd |
|      | 00227 |
+---+ +---] [---+
|      |      |
|      | O_Dtcd1 |
|      | 00228 |
+---+ +---] [---+
|      |      |
|      | O_Dtcd2 |
|      | 00229 |
+---+ +---] [---+
|

```

GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

: << RUNG 71 >>
:
: *****
: *
: * If the Command Byte is non-zero and is not a Zero Data Byte *
: * Command the following rung of logic moves the 1st and 2nd *
: * Data Bytes out of the Register Table and into Data Byte *
: * Storage Register R22. *
: * *
: * O205 O_RgVal Zero Value In Register Detected *
: * O230 O_Dtcd3 Flag 3_Zero Data Byte Detected *
: * R22 Srtch_7 Scratch Register/1st and 2nd Data Bytes *
: * R23 3rd_DB Storage For 3rd Data *
: * *
: *****
: O_Dtcd O_Dtcd3 Reg_Ptr Srtch_7
: O0205 O0230 R0024 R0022 Const ( )
+---]/[-----]/[---[TABLE-T0-DEST LEN]-----]
: O40
:
: << RUNG 72 >>
:
: *****
: *
: * If the Command Byte is non-zero and is not a Zero Data Byte *
: * Command the 3rd Data Byte is transferred from the Register *
: * Table to R23. If the pointer (R24) rests at the last register *
: * in the table O232 is energized which terminates the download *
: * subroutine. *
: * *
: * O205 O_RgVal Zero Value In Register Detected *
: * O230 O_Dtcd3 Flag 3_Zero Data Byte Detected *
: * R23 3rd_DB Storage For 3rd Data Byte *
: * R24 Reg_Ptr Pointer For Register Table *
: * *
: *****
: O_Dtcd O_Dtcd3 Reg_Ptr 3rd_DB E0Tble2
: O0205 O0230 R0024 R0023 Const O0232
+---]/[-----]/[---[TABLE-T0-DEST LEN]-----]
: O40
  
```

GE SERIES SIX DOCUMENTATION
 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

  << RUNG 73 >>
  *****
  *
  *      If the Command Byte is non-zero the Command located in
  *      R21 with data (R22 and R23) are downloaded to the HSC.
  *
  *      033      CmdByte      HSC Command Byte
  *      041      DatByt1     HSC 1st Data Byte/and 2nd Data Byte
  *      057      DatByt3     HSC 3rd Data Byte
  *      R21      Stor_CB     Storage For Command Byte
  *      R22      Srtch_7     Scratch Register/1st and 2nd Data Bytes
  *
  *****
  O_Dtcd  Stor_CB CmdByte Srtch_7 DatByt1 3rd_DB      DatByt3
  00205  R0021  00033  R0022  00041  R0023      00057
  +---] / [---[ REG TO I/O ]-[ REG TO I/O ]-[ MOVE RIGHT 8 BITS ]- ( )

  << RUNG 74 >>
  +[NO OP]- ( )

  << RUNG 75 >>
  *****
  *
  *      If CB = 35 Simulator LED Outputs 013 to 016 are updated to
  *      reflect their corresponding Preset Comparison Senses.
  *
  *      013      01CmpSe     HSC Output 1 Preset Comparison Sense
  *      014      02CmpSe     HSC Output 2 Preset Comparison Sense
  *      015      03CmpSe     HSC Output 3 Preset Comparison Sense
  *      016      04CmpSe     HSC Output 4 Preset Comparison Sense
  *      049      DatByt2     HSC 2nd Data Byte/Bit 17
  *      050      Dsct_18     Discrete Data_HSC Output Bit 18
  *      051      Dsct_19     Discrete Data_HSC Output Bit 19
  *      052      Dsct_20     Discrete Data_HSC Output Bit 20
  *      0205     O_RqVal     Zero Value In Register Detected
  *      0230     O_Dtcd3     Flag 3_Zero Data Byte Detected
  *      0233     UpDtOut     If CB=35 Update Corresponding Outputs
  *
  *****
  O_Dtcd  O_Dtcd3      Srtch_1 Srtch_1 Stor_CB      UpDtOut
  00205  00230  Const      R0012  R0012  R0021      00233
  +---] / [---[ A      MOVE      B ]-[ A : B ]----- (05)
  |
  |      +00035
  
```

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 SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
 REGISTER TABLE METHOD

```

| << RUNG 76 >>
|UpDtOut DatByt2                                01CmpSe
| 00233 00049                                00013
+--] [-----] [-----] [LATCH]---- ( L )
|
|UpDtOut DatByt2                                ( )
| 00233 00049                                ( )
+--] [-----] / [-----] (UL)
|
| << RUNG 77 >>
|UpDtOut Dsct_18                                02CmpSe
| 00233 00050                                00014
+--] [-----] [-----] [LATCH]---- ( L )
|
|UpDtOut Dsct_18                                ( )
| 00233 00050                                ( )
+--] [-----] / [-----] (UL)
|
| << RUNG 78 >>
|UpDtOut Dsct_19                                03CmpSe
| 00233 00051                                00015
+--] [-----] [-----] [LATCH]---- ( L )
|
|UpDtOut Dsct_19                                ( )
| 00233 00051                                ( )
+--] [-----] / [-----] (UL)
|
| << RUNG 79 >>
|UpDtOut Dsct_20                                04CmpSe
| 00233 00052                                00016
+--] [-----] [-----] [LATCH]---- ( L )
|
|UpDtOut Dsct_20                                ( )
| 00233 00052                                ( )
+--] [-----] / [-----] (UL)
|
| << RUNG 80 >>
+ [ Return ] -

```

GE SERIES SIX DOCUMENTATION
SERIES SIX HIGH SPEED COUNTER DATA DOWNLOAD PROGRAM
REGISTER TABLE METHOD

```
| << RUNG 81 >>  
|  
+ [ENDSW]-  
| << RUNG 82 >>  
+ [ENDSW]-  
|
```

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ORDERING INFORMATION

<u>Equipment</u>	<u>Catalog Number</u>
Circuit Board without Faceplate	IC600YB827A
Faceplate	IC600FP827A
Circuit Board with Faceplate	IC600BF827A

CATALOG NUMBER REVISION SUFFIX

The equipment listed above having the catalog numbers shown and the same equipment having a higher alpha suffix is designed for listing by UL for use as auxiliary control devices. The equipment is a direct replacement for equipment having the same catalog number but a lower alpha suffix.

The UL symbol on the nameplate means the product is listed by Underwriters Laboratories Inc. (UL Standard No. 508, Industrial Control Equipment, subsection Electronic Power Conversion Equipment.)

For further information, contact your local GE Fanuc sales office.

GE FANUC AUTOMATION NORTH AMERICA, INC., CHARLOTTESVILLE, VIRGINIA

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