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GE Fanuc Automation

Programmable Control Products

IC697VAL306 12-bit Analog Output Board

User's Manual

GFK-2078

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May 2002

Warnings, Cautions, and Notes as Used in this Publication

Warning

Warning notices are used in this publication to emphasize that hazardous voltages, currents, temperatures, or other conditions that could cause personal injury exist in this equipment or may be associated with its use.

In situations where inattention could cause either personal injury or damage to equipment, a Warning notice is used.

Caution

Caution notices are used where equipment might be damaged if care is not taken.

Note

Notes merely call attention to information that is especially significant to understanding and operating the equipment.

This document is based on information available at the time of its publication. While efforts have been made to be accurate, the information contained herein does not purport to cover all details or variations in hardware or software, nor to provide for every possible contingency in connection with installation, operation, or maintenance. Features may be described herein which are not present in all hardware and software systems. GE Fanuc Automation assumes no obligation of notice to holders of this document with respect to changes subsequently made.

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CIMSTAR	Modelmaster	Series 90	VersaPro
Field Control	Motion Mate	Series Five	VuMaster
GEnet	ProLoop	Series One	Workmaster

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Chapter 1

Introduction, Description, and Specifications

This manual describes the installation and operation of the IC697VAL306 12-bit Analog Output Board.

Reference Material and Other GE Fanuc Manuals

For a detailed explanation of the VMEbus and its characteristics, the publication “The VMEbus Specification” is available from:

VITA
VMEbus International Trade Association
7825 East Gelding Dr., No. 104
Scottsdale, AZ 85260
(480) 951-8866
FAX: (480) 951-0720
Internet: www.vita.com

The following Application and Configuration Guides are available from GE Fanuc to assist in the selection, specification, and implementation of systems based upon GE Fanuc’s products:

Analog I/O Products (Built-in-Test) Configuration Guide (catalog number GFK-2084)	Provides assistance in configuring analog I/O subsystems based on GE Fanuc’s analog I/O products, including common designs, which offer a wide variety of solutions.
Connector and I/O Cable Application Guide (catalog number GFK-2085)	Describes I/O connections that can be used with GE Fanuc’s VMEbus products. Includes connector compatibility information and examples.

General Description

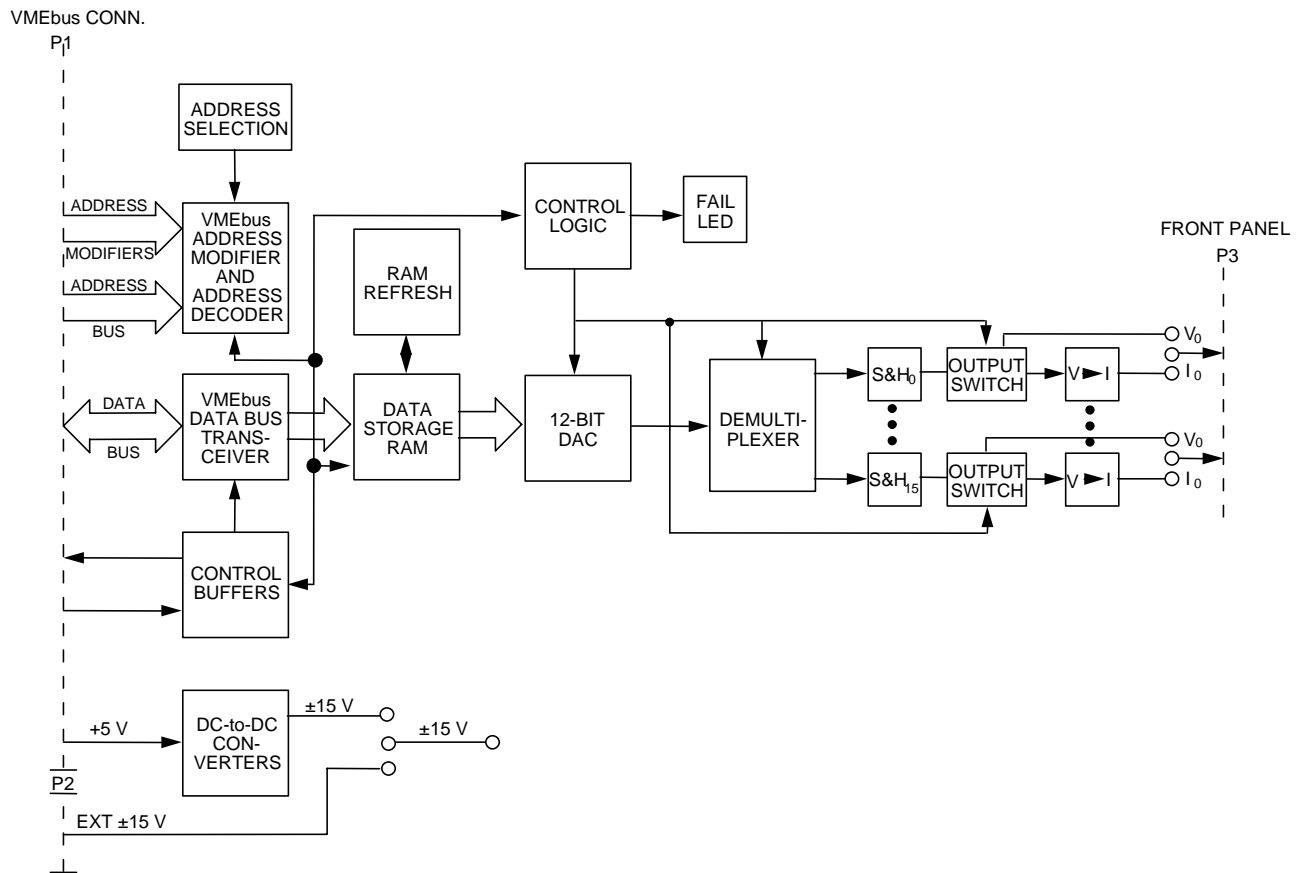
The 12-bit Analog Output Board provides 16 high-quality analog output channels. These channels are jumper-selectable for voltage outputs, current loop outputs, or a combination of voltage and current loop outputs. Each output current range is also jumper-selectable. On-board ± 15 V DC-to-DC converters are used to supply ± 15 V. The following brief overview of principal features illustrates the flexibility and the performance that is available with the 12-bit Analog Output Board:

- 16 analog output channels
- Jumper-selectable voltage or current outputs
- 12-bit DAC resolution
- Output current ranges of 4 to 20 mA, 0 to 20 mA, and 5 to 25 mA (4 to 12 mA, 0 to 10 mA, and 5 to 15 mA are also available)
- Output voltage ranges of ± 2.5 V, ± 5.0 V, ± 10 V, 0 to + 10 V, and 0 to + 5 V
- Output short-circuit protection
- Front panel outputs (P3)
- Front panel Fail LED indicator
- Double height Eurocard form factor

Functional Description

Each of the 16 channels in the self-contained, 12-bit Analog Output Board is programmable by the user via 16 12-bit RAM locations. Each RAM location corresponds to an output channel. The 12-bit Analog Output Board periodically fetches the 12-bit binary values out of the RAM locations and uses them as the inputs to the on-board DAC. The output of the DAC is distributed to the sample-and-hold circuits associated with each output channel.

Figure 1-1: 12-bit Analog Output Board Functional Block Diagram



Safety Summary

The following general safety precautions must be observed during all phases of this operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product. GE Fanuc assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to GE Fanuc for service and repair to ensure that safety features are maintained.

Chapter 2

Configuration and Installation

This chapter, divided into the following sections, provides configuration and installation instructions for the 12-bit Analog Output Board:

- Physical Installation
- Before Applying Power: Checklist
- Operational Configuration
- Calibration
- Connector Descriptions

Caution

Some of the components assembled on GE Fanuc's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. Unused boards should be stored in the same protective boxes in which they were shipped. When the board is to be laid on a bench for configuring, etc., it is suggested that conductive material be inserted under the board to provide a conductive shunt.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to GE Fanuc together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation

Caution

Do not install or remove boards while power is applied.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

Before Applying Power: Checklist

Before installing the board in a VMEbus system, check the following items to ensure that the board is ready for the intended application.

- Have the chapters pertaining to programming and theory, chapters 3 and 4, been reviewed and applied to system requirements?
- Review “Factory Installed Jumpers” on page 2-4 and Table 2-1 on page 2-5 to verify that all factory installed jumpers are in place. To change the board address or address modifier response, refer to “Board Address and Address Modifier Selection” on page 2-4.
- Have the I/O cables, with the proper mating connectors, been connected to the input/output connector P3? Refer to “Connector Descriptions” on page 2-18 for a description of the P3 connector.
- Calibration has been performed at the factory. If recalibration should be required, refer to “Calibration” on page 2-8.

Operational Configuration

Control of the 12-bit Analog Output Board address and I/O access mode are determined by field replaceable, on-board jumpers. This section describes the use of these jumpers, and their effects on board performance. The locations and functions of all 12-bit Analog Output Board jumpers are shown in Figure 2-1 on page 2-6 and Table 2-1 on page 2-5, respectively.

Factory Installed Jumpers

Each 12-bit Analog Output Board is configured at the factory with the specific jumper arrangement shown in Table 2-1 on page 2-5. The factory configuration establishes the following functional baseline for the 12-bit Analog Output Board, and ensures that all essential jumpers are installed.

- Board short address is set at 0000 HEX
- I/O access mode is short nonprivileged
- Current loop outputs on all channels
- 4 to 20 mA current range on all channels

Board Address and Address Modifier Selection

Jumper J20, and jumpers J22 and J23 permit the 12-bit Analog Output Board to be located on any 64-byte boundary within the short I/O address space. The short I/O address space consists of all addresses between NNNN0000 HEX* and NNNNFFFF HEX, and requires that 15 (word) address lines be decoded in order to account for all locations. Since five lines are used for decoding on-board functions (A1 through A5), the 12-bit Analog Output Board address is defined by ten lines; address bits A06 through A15.

The board address is programmed by installing shorting plugs at all "zero" or LOW address bit jumper positions, and by omitting the shorting plugs at the "one" or HIGH positions. Address bit A06 has a weight of 64-byte locations. As an example, the jumper arrangement shown in Table 2-2 on page 2-7 would produce a board address of NNNN8840 HEX.

I/O access mode is programmed by selecting address modifier AM2 with jumper J21. Short supervisory access is selected by omitting the jumper. Short nonprivileged access is selected by installing the jumper.

* The value NNNN depends on the make and model of CPU board used.

Table 2-1: Programmable Jumper Functions

Jumper	Function	Factory Configured **
J20 – 1, 2	Board Address Bit A15 = 0	Installed
J20 – 3, 4	Board Address Bit A14 = 0	Installed
J20 – 5, 6	Board Address Bit A13 = 0	Installed
J20 – 7, 8	Board Address Bit A12 = 0	Installed
J20 – 9, 10	Board Address Bit A11 = 0	Installed
J20 – 11, 12	Board Address Bit A10 = 0	Installed
J20 – 13, 14	Board Address Bit A09 = 0	Installed
J20 – 15, 16	Board Address Bit A08 = 0	Installed
J23 – 1, 2	Board Address Bit A07 = 0	Installed
J22 – 1, 2	Board Address Bit A06 = 0	Installed
J21 – 1, 2	Short Supervisory Access	Omitted
J19 – 1, 2	“8 CH L” (Not Used)	Omitted
J18 – 1, 2	Unipolar Operation	Installed
J18 – 2, 3	Bipolar Operation	Omitted
J17 – 1, 2 *	10 V Full Scale Range	Installed
J17 – 2, 3 *	5 V Full Scale Range	Omitted
J1 through J16	See Figure 2-2 on page 2-8	

* The J17 jumper is omitted for the 20 V FSR.

** The factory configuration shown is for the -000 option of the 12-bit Analog Output Board.

Figure 2-1: Locations of Programmable Jumpers, Adjustment Potentiometer, and Test Points

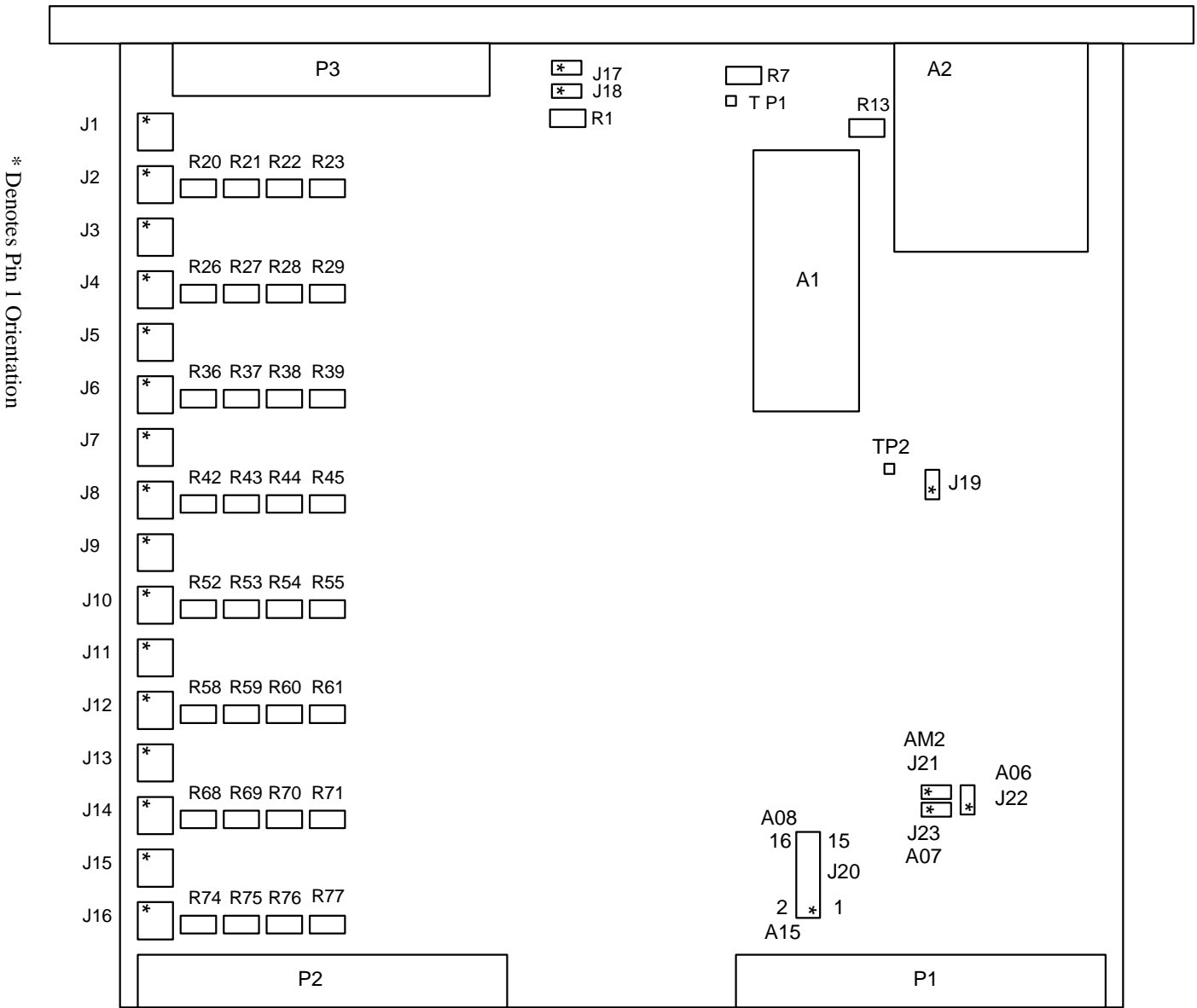


Table 2-2: Example Board Address (NNNN9980 HEX) Selection

Jumper	Address Bit	State *
J22 – 1, 2	A06	Open
J23 – 1, 2	A07	Shorted
J20 – 15, 16	A08	Shorted
J20 – 13, 14	A09	Shorted
J20 – 11, 13	A10	Shorted
J20 – 9, 10	A11	Open
J20 – 7, 8	A12	Shorted
J20 – 5, 6	A13	Shorted
J20 – 3, 4	A14	Shorted
J20 – 1, 2	A15	Open

* Shorted = “zero” (Jumper installed).
Open = “one”.

Analog Voltage Output Mode

Figure 2-2 on page 2-8 shows how to configure each individual channel for voltage output mode.

Output Voltage Range

Output voltage range is controlled by jumper J17. The maximum full scale range is 20 V. To modify the full scale range to 10 V or 5 V, configure jumper J17 as indicated in Table 2-1 on page 2-5. The 20 V full scale range is selected by omitting the J17 jumper entirely.

Bipolar or Unipolar Operation

Bipolar or Unipolar operation of the analog voltage outputs is selected with jumper J18, as indicated in Table 2-1 on page 2-5.

Analog Current Output Mode

Figure 2-2 on page 2-8 shows how to configure each individual channel for current output mode at any of the specified ranges. In order to produce current loop outputs, the voltage outputs must be configured for unipolar operation. Typically the voltage range is set to 0 to +10 V to produce 4 to 20 mA, 0 to 20 mA or 5 to 25 mA. A voltage range of 0 to +5 V can be selected to produce 4 to 12 mA, 0 to 10 mA or 5 to 15 mA.

Calibration

Before delivery from the factory, the 12-bit Analog Output Board is fully calibrated and conforms to all specifications. Should recalibration be required, however, perform the procedures in “Analog Outputs Calibration Procedure” on page 2-10 with the equipment listed in “Equipment Required” on page 2-9. The locations of all adjustments and test points are shown in Figure 2-1 on page 2-6. Adjustment potentiometers and their functions are listed in the Table 2-3 on page 2-9.

As delivered from the factory, all calibration adjustments are sealed against accidental movement. The seals are easily broken for recalibration, however. All adjustments should be resealed with a suitable fast-curing sealing compound after recalibration has been completed.

Caution

Do not install or remove this board with power applied to the system.

Figure 2-2: Output Channel Jumper Configurations - Jumper Connections for J1 through J16

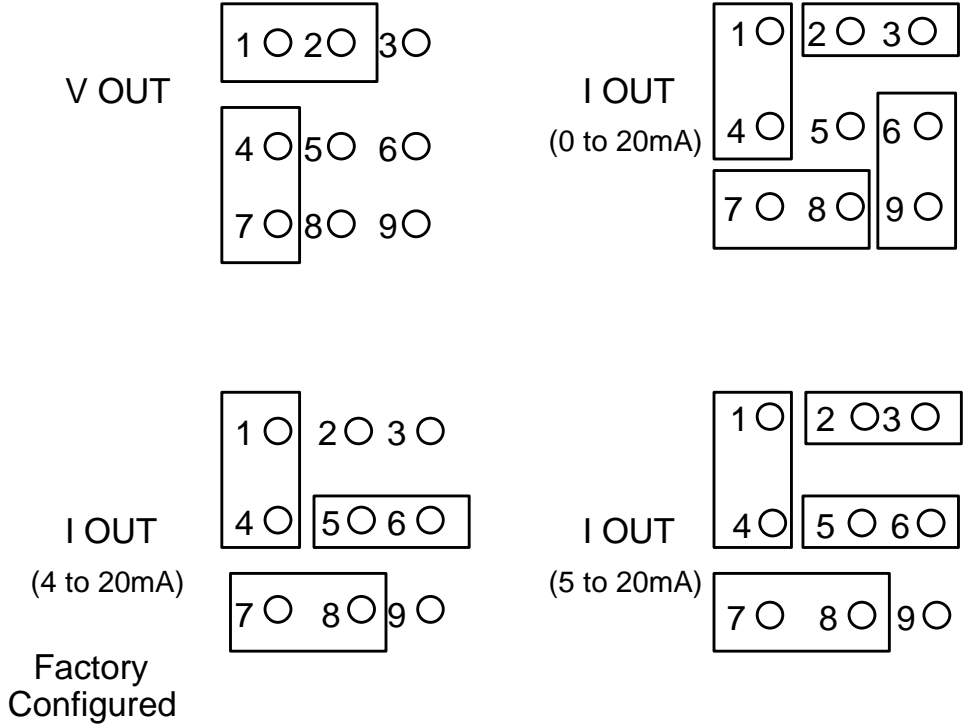


Table 2-3: Adjustment Potentiometer Functions

Channel Number	Zero Adjust	Span Adjust	
0	R21	R20	Current Adjustments
1	R23	R22	
2	R27	R26	
3	R29	R28	
4	R37	R36	
5	R39	R38	
6	R43	R42	
7	R45	R44	
8	R53	R52	
9	R55	R54	
10	R59	R58	
11	R61	R60	
12	R69	R68	
13	R71	R70	
14	R75	R74	
15	R77	R76	
R1	Bipolar Outputs Zero Adjust		Voltage Adjustments
R7	Outputs Gain Adjust		
R13	Unipolar Outputs Zero Adjust		

Equipment Required

- **Digital Multimeter (DMM)** – ± 1.0000 VDC and ± 10.000 VDC ranges; 5 or more digits; ± 0.005 percent of reading voltage measurement accuracy; $10\text{ M}\Omega$ minimum input impedance. Current measurements at $1\ \mu\text{A}$ resolution; 5 or more digits.
- **Chassis** – VMEbus backplane or equivalent, J1 and J2 connectors, VMEbus master controller, $+5 \pm 0.1$ VDC, power supply. One slot allocated for testing the 12-bit Analog Output Board.
- **Extender board** – VMEbus extender board.
- **Test cables** – Test cables for the equipment listed above.

Analog Outputs Calibration Procedure

The following sections provide detailed calibration procedures for all of the voltage/current ranges provided by the 12-bit Analog Output Board.

- Calibration Procedure for 0 to 10 V Output Range
- Calibration Procedure for 0 to 5 V Output Range
- Calibration Procedure for ± 2.5 V Output Range
- Calibration Procedure for ± 5.0 V Output Range
- Calibration Procedure for ± 10.0 V Output Range
- Calibration Procedure for 4 to 20 mA Output Range
- Calibration Procedure for 0 to 20 mA Output Range
- Calibration Procedure for 5 to 25 mA Output Range

The following procedures are performed with the FAIL LED L bit set to a "one", the TWO'S COMPL L bit set to a "one", and the FAST REFRESH H bit set to a "zero" in the CSR.

Note

Calibration of outputs to a specific range does not necessarily mean that if the jumpers are reconfigured, this channel will still be calibrated.

Calibration Procedure for 0 to 10 V Output Range

Setup:

1. Install the 12-bit Analog Output Board on an extender board in a VMEbus backplane.
2. Configure all output channels for voltage outputs (see Figure 2-2 on page 2-8).
3. Configure J17 and J18 for unipolar operation and 10 V full scale range (see Table 2-1 on page 2-5).
4. Turn ON the power to the VMEbus backplane.

DAC Output Adjustments:

5. Write 5800 HEX to relative address 02.
6. Connect the (+) lead of the DMM to Test Point No. 1 (TP1).
Connect the (-) lead of the DMM to TP2.
7. Write 0000 to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
8. Adjust potentiometer R13 for a DMM indication of 0.0000 ± 0.0010 VDC.
9. Write 0FFF to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).

10. Adjust potentiometer R7 for a DMM indication of $+9.9976 \pm 0.0010$ VDC .
11. Gain adjustments (Steps 9 and 10) may appreciably alter the offset adjustment and vice versa; therefore, Steps 7 through 10 must be repeated as many times as required.
12. Calibration of the analog outputs is completed. Remove power and all test connections.

Calibration Procedure for 0 to 5 V Output Range

Setup:

1. Install the 12-bit Analog Output Board on an extender board in a VMEbus backplane.
2. Configure all output channels for voltage outputs (see Figure 2-2 on page 2-8).
3. Configure J17 and J18 for unipolar operation and 5 V full scale range (see Table 2-1 on page 2-5).
4. Turn ON the power to the VMEbus backplane.

DAC Output Adjustments:

5. Write 5800 HEX to relative address 02.
6. Connect the (+) lead of the DMM to Test Point No. 1 (TP1).
Connect the (-) lead of the DMM to TP2.
7. Write 0000 to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
8. Adjust potentiometer R13 for a DMM indication of 0.0000 ± 0.0010 VDC.
9. Write 0FFF to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
10. Adjust potentiometer R7 for a DMM indication of $+4.9988 \pm 0.0010$ VDC .
11. Gain adjustments (Steps 9 and 10) may appreciably alter the offset adjustment and vice versa; therefore, Steps 7 through 10 must be repeated as many times as required.
12. Calibration of the analog outputs is completed. Remove power and all test connections.

Calibration Procedure for ± 2.5 V Output Range

Setup:

1. Install the 12-bit Analog Output Board on an extender board in a VMEbus backplane.
2. Configure all output channels for voltage outputs (see Figure 2-2 on page 2-8).
3. Configure J17 and J18 for bipolar operation and 5 V full scale range (see Table 2-1 on page 2-5).
4. Turn ON the power to the VMEbus backplane.

DAC Output Adjustments:

5. Write 5800 HEX to relative address 02.
6. Connect the (+) lead of the DMM to Test Point No. 1 (TP1).
Connect the (-) lead of the DMM to TP2.
7. Write 0800 to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
8. Adjust potentiometer R1 for a DMM indication of 0.0000 ± 0.0010 VDC.
9. Write 0FFF to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
10. Adjust potentiometer R7 for a DMM indication of $+2.4988 \pm 0.0010$ VDC .
11. Gain adjustments (Steps 9 and 10) may appreciably alter the offset adjustment and vice versa; therefore, Steps 7 through 10 must be repeated as many times as required.
12. Calibration of the analog outputs is completed. Remove power and all test connections.

Calibration Procedure for ± 5.0 V Output Range

Setup:

1. Install the 12-bit Analog Output Board on an extender board in a VMEbus backplane.
2. Configure all output channels for voltage outputs (see Figure 2-2 on page 2-8).
3. Configure J17 and J18 for bipolar operation and 10 V full scale range (see Table 2-1 on page 2-5).
4. Turn ON the power to the VMEbus backplane.

DAC Output Adjustments:

5. Write 5800 HEX to relative address 02.
6. Connect the (+) lead of the DMM to Test Point No. 1 (TP1).
Connect the (-) lead of the DMM to TP2.
7. Write 0800 to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
8. Adjust potentiometer R1 for a DMM indication of 0.0000 ± 0.0010 VDC.
9. Write 0FFF to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
10. Adjust potentiometer R7 for a DMM indication of $+4.9976 \pm 0.0010$ VDC .
11. Gain adjustments (Steps 9 and 10) may appreciably alter the offset adjustment and vice versa; therefore, Steps 7 through 10 must be repeated as many times as required.
12. Calibration of the analog outputs is completed. Remove power and all test connections.

Calibration Procedure for ± 10.0 V Output Range

Setup:

1. Install the 12-bit Analog Output Board on an extender board in a VMEbus backplane.
2. Configure all output channels for voltage outputs (see Figure 2-2 on page 2-8).
3. Configure J17 and J18 for bipolar operation and 20 V full scale range (see Table 2-1 on page 2-5).
4. Turn ON the power to the VMEbus backplane.

DAC Output Adjustments:

5. Write 5800 HEX to relative address 02.
6. Connect the (+) lead of the DMM to Test Point No. 1 (TP1).
Connect the (-) lead of the DMM to TP2.
7. Write 0800 to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
8. Adjust potentiometer R1 for a DMM indication of 0.0000 ± 0.0010 VDC.
9. Write 0FFF to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
10. Adjust potentiometer R7 for a DMM indication of $+9.9951 \pm 0.0010$ VDC .
11. Gain adjustments (Steps 9 and 10) may appreciably alter the offset adjustment and vice versa; therefore, Steps 7 through 10 must be repeated as many times as required.
12. Calibration of the analog outputs is completed. Remove power and all test connections.

Calibration Procedure for 4 to 20 mA Output Range

Setup:

1. Install the 12-bit Analog Output Board on an extender board in a VMEbus backplane.
2. Configure all output channels for 4 to 20 mA (see Figure 2-2 on page 2-8).
3. Configure J17 and J18 for unipolar operation and 10 V full scale range (see Table 2-1 on page 2-5).
4. Turn ON the power to the VMEbus backplane.

DAC Output Adjustments:

5. Write 5C00 HEX to relative address 02.
6. Connect the (+) lead of the DMM to Test Point No. 1 (TP1).
Connect the (-) lead of the DMM to TP2.
7. Write 0000 to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
8. Adjust potentiometer R13 for a DMM indication of 0.0000 ± 0.0010 VDC.
9. Write 0FFF to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
10. Adjust potentiometer R7 for a DMM indication of $+9.9976 \pm 0.0010$ VDC .
11. Gain adjustments (Steps 9 and 10) may appreciably alter the offset adjustment and vice versa; therefore, Steps 7 through 10 must be repeated as many times as required.

Current Output Adjustments:

12. Set the DMM for current measurements (make sure that the DMM is set to a range that provides a 1 μ A or better resolution).
13. Connect the (+) lead of the DMM to "CH 0 OUT" (P3-A1). Connect the (-) lead of the DMM to "AGND" (P3-A1). See the Table 2-5 on page 2-22 for P3 connector pin assignments.
14. Write 0000 to relative address 20 HEX. See Table 3-1 on page 3-4 for the 12-bit Analog Output Board memory map.
15. Adjust potentiometer R21 (offset adjustment potentiometer) for a DMM indication of 4.000 ± 0.001 mA.
16. Write 0FFF to relative addresses 20 HEX (i.e. the memory location corresponding to channel 0).
17. Adjust potentiometer R20 (span adjustment potentiometer) for a DMM indication of 19.996 ± 0.002 mA.

18. Span adjustments (Steps 16 and 17) may appreciably alter the offset adjustment and vice versa; therefore, Steps 14 through 17 must be repeated as many times as required.
19. Repeat Steps 13 through 18 for channels 1 through 15. See Table 3-1 on page 3-4 for a memory map of the 12-bit Analog Output Board. See Table 2-3 on page 2-9 for a list of all the adjustment potentiometers, their functions and associated channel numbers.
20. Calibration of the analog outputs is completed. Remove power and all test connections.

Calibration Procedure for 0 to 20 mA Output Range

Setup:

1. Install the 12-bit Analog Output Board on an extender board in a VMEbus backplane.
2. Configure all output channels for 0 to 20 mA (see Figure 2-2 on page 2-8).
3. Configure J17 and J18 for unipolar operation and 10 V full scale range (see Table 2-1 on page 2-5).
4. Turn ON the power to the VMEbus backplane.

DAC Output Adjustments:

5. Write 5C00 HEX to relative address 02.
6. Connect the (+) lead of the DMM to Test Point No. 1 (TP1).
Connect the (-) lead of the DMM to TP2.
7. Write 0000 to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
8. Adjust potentiometer R13 for a DMM indication of 0.0000 ± 0.0010 VDC.
9. Write 0FFF to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
10. Adjust potentiometer R7 for a DMM indication of $+9.9976 \pm 0.0010$ VDC .
11. Gain adjustments (Steps 9 and 10) may appreciably alter the offset adjustment and vice versa; therefore, Steps 7 through 10 must be repeated as many times as required.

Current Output Adjustments:

12. Set the DMM for current measurements (make sure that the DMM is set to a range that provides a 1 μ A or better resolution).
13. Connect the (+) lead of the DMM to "CH 0 OUT" (P3-A1). Connect the (-) lead of the DMM to "AGND" (P3-A1). See Table 2-5 on page 2-22 for P3 connector pin assignments.
14. Write 0001 to relative address 20 HEX. See Table 3-1 on page 3-4 for the 12-bit Analog Output Board memory map.
15. Adjust potentiometer R21 (offset adjustment potentiometer) for a DMM indication of 0.005 ± 0.001 mA.
16. Write 0FFF to relative addresses 20 HEX (i.e. the memory location corresponding to channel 0).
17. Adjust potentiometer R20 (span adjustment potentiometer) for a DMM indication of 19.995 ± 0.002 mA.
18. Span adjustments (Steps 16 and 17) may appreciably alter the offset adjustment and vice versa; therefore, Steps 14 through 17 must be repeated as many times as required.
19. Repeat Steps 13 through 18 for channels 1 through 15. See Table 3-1 on page 3-4 for a memory map of the 12-bit Analog Output Board. See Table 2-3 on page 2-9 for a list of all the adjustment potentiometers, their functions and associated channel numbers.
20. Calibration of the analog outputs is completed. Remove power and all test connections.

Calibration Procedure for 5 to 25 mA Output Range

Setup:

1. Install the 12-bit Analog Output Board on an extender board in a VMEbus backplane.
2. Configure all output channels for 5 to 25 mA (see Figure 2-2 on page 2-8).
3. Configure J17 and J18 for unipolar operation and 10 V full scale range (see Table 2-1 on page 2-5).
4. Turn ON the power to the VMEbus backplane.

DAC Output Adjustments:

5. Write 5C00 HEX to relative address 02.
6. Connect the (+) lead of the DMM to Test Point No. 1 (TP1).
Connect the (-) lead of the DMM to TP2.
7. Write 0000 to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).

8. Adjust potentiometer R13 for a DMM indication of 0.0000 ± 0.0010 VDC.
9. Write 0FFF to relative addresses 20 HEX through 3E HEX (i.e. the 16 decimal memory locations corresponding to the 16 output channels).
10. Adjust potentiometer R7 for a DMM indication of $+9.9976 \pm 0.0010$ VDC .
11. Gain adjustments (Steps 9 and 10) may appreciably alter the offset adjustment and vice versa; therefore, Steps 7 through 10 must be repeated as many times as required.

Current Output Adjustments:

12. Set the DMM for current measurements (make sure that the DMM is set to a range that provides a $1 \mu\text{A}$ or better resolution).
13. Connect the (+) lead of the DMM to "CH 0 OUT" (P3-A1). Connect the (-) lead of the DMM to "AGND" (P3-A1). See Table 2-5 on page 2-22 for P3 connector pin assignments.
14. Write 0000 to relative address 20 HEX. See Table 3-1 on page 3-4 for the 12-bit Analog Output Board memory map.
15. Adjust potentiometer R21 (offset adjustment potentiometer) for a DMM indication of 5.000 ± 0.001 mA.
16. Write 0FFF to relative addresses 20 HEX (i.e. the memory location corresponding to channel 0).
17. Adjust potentiometer R20 (span adjustment potentiometer) for a DMM indication of 24.995 ± 0.002 mA.
18. Span adjustments (Steps 16 and 17) may appreciably alter the offset adjustment and vice versa; therefore, Steps 14 through 17 must be repeated as many times as required.
19. Repeat Steps 13 through 18 for channels 1 through 15. See Table 3-1 on page 3-4 for a memory map of the 12-bit Analog Output Board. See Table 2-3 on page 2-9 for a list of all the adjustment potentiometers, their functions and associated channel numbers.
20. Calibration of the analog outputs is completed. Remove power and all test connections.

Connector Descriptions

Three connectors, P1, P2, and P3 (Figure 2-1 on page 2-6), provide all connections to the 12-bit Analog Output Board. P1 contains the address, data and control lines, and all additional signals necessary to control VMEbus functions related to the board. P2 provides additional VMEbus power and ground connections as well as the external power connections. P3 provides the connections for the 16 analog output channels.

Orientation of the P2 connector is shown in the Figure 2-3 on 2-19, and the P2 signal assignments are listed in Table 2-4 on page 2-20.

Orientation of the P3 connector is shown in Figure 2-4 on page 2-21, and the P3 signal assignments are listed in Table 2-5 on page 2-22. The mating connector for P3 (Panduit Model 120-332-435E or equivalent) is designed to be used with a standard 32-wire ribbon-cable with a conductor spacing of 0.050 inches. A twisted-pair ribbon cable with an overall shield is recommended for applications involving low level signals in high electrical noise environments.

Figure 2-3: P1/P2 Connector – Pin Assignments

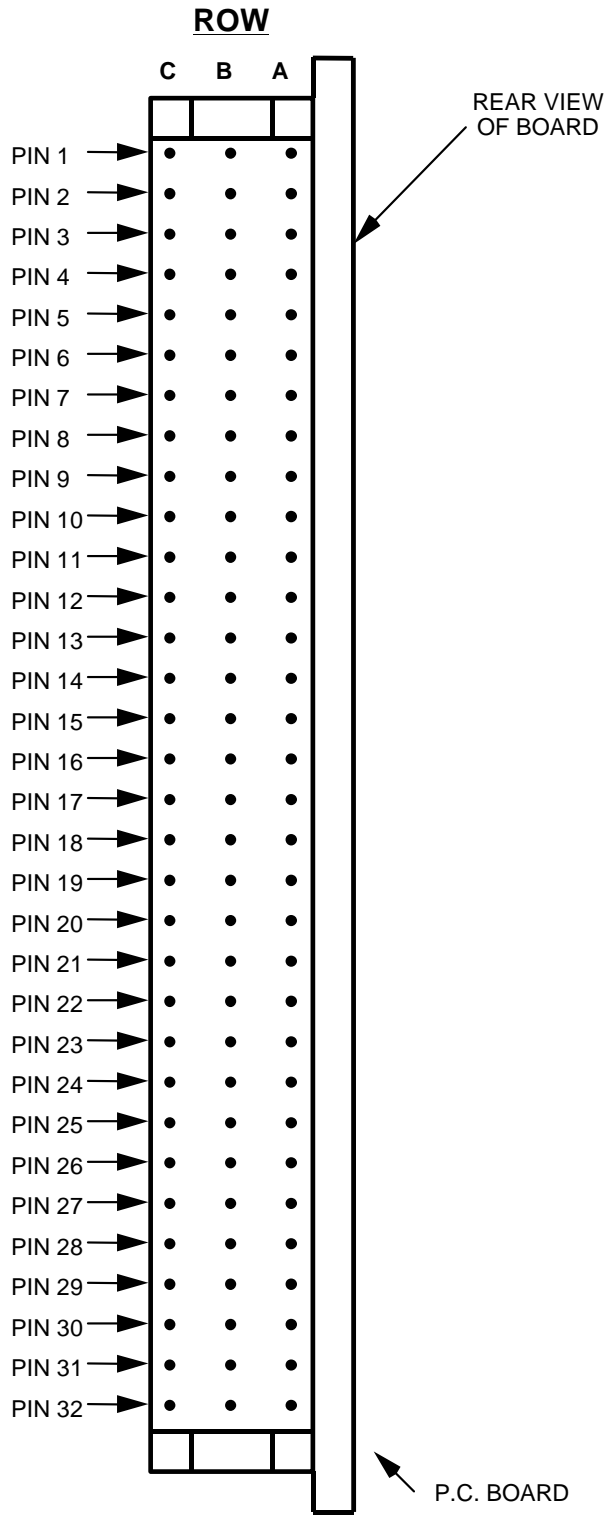


Table 2-4: P2 Connector Signal Assignments

Pin No.	A	B	C
1		+5 V	
2		GND	
3			
4			
5			
6			
7			
8			
9			
10			
11			
12		GND	
13		+5 V	
14			
15			
16			
17			
18			
19			
20			
21			
22		GND	
23			
24			
25	EXT +15 V		
26	EXT +15 V		
27			
28	EXT ANA COM		
29	EXT ANA COM		
30			
31	EXT -15 V	GND	
32	EXT -15 V	+5 V	

Figure 2-4: P3 Connector – Pin Configuration

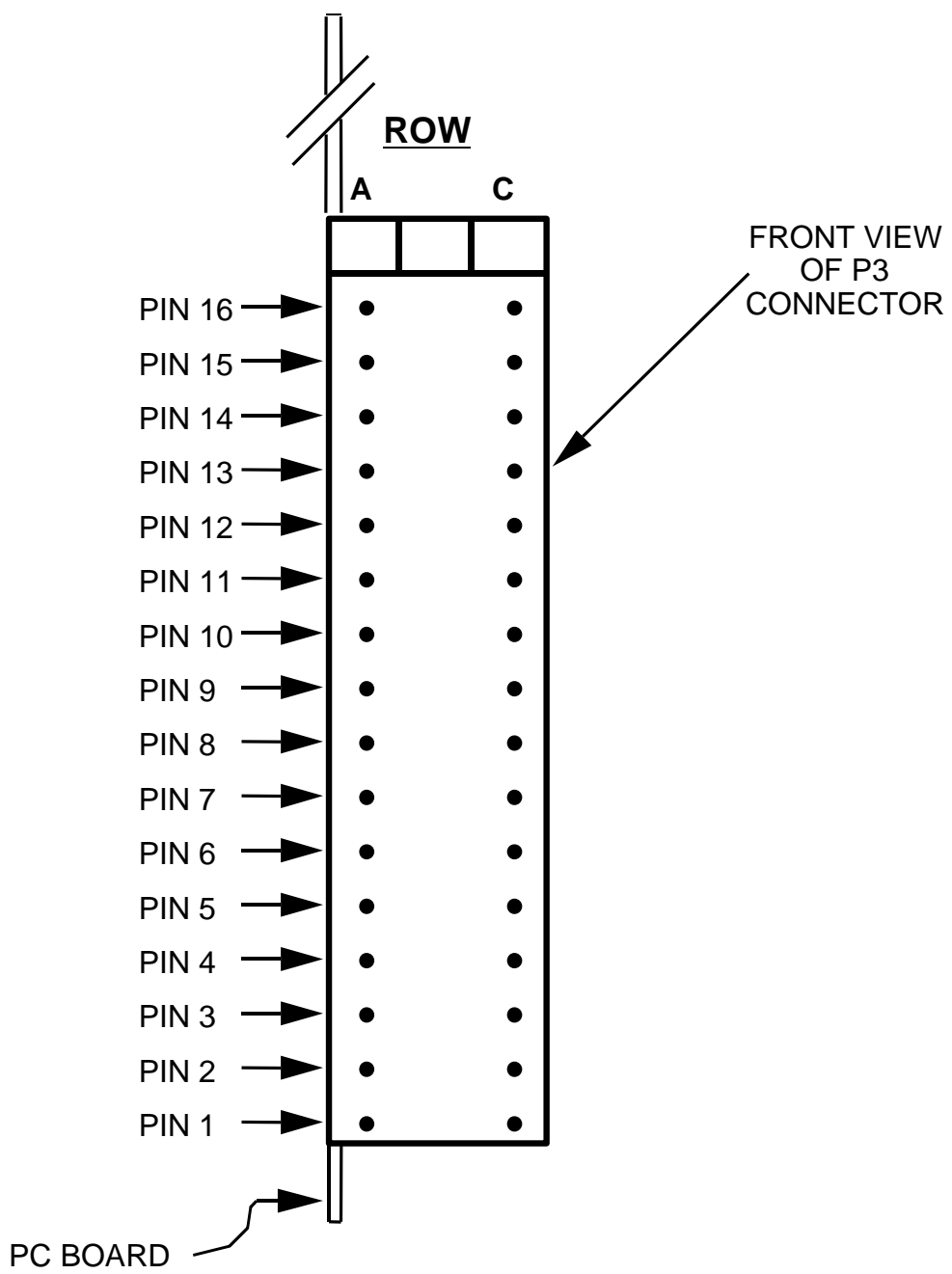


Table 2-5: P3 Connector Pin Assignments

Pin No.	A	C
16	CH15 OUT	AGND
15	CH14 OUT	AGND
14	CH13 OUT	AGND
13	CH12 OUT	AGND
12	CH11 OUT	AGND
11	CH10 OUT	AGND
10	CH9 OUT	AGND
9	CH8 OUT	AGND
8	CH7 OUT	AGND
7	CH6 OUT	AGND
6	CH5 OUT	AGND
5	CH4 OUT	AGND
4	CH3 OUT	AGND
3	CH2 OUT	AGND
2	CH1 OUT	AGND
1	CH0 OUT	AGND

Chapter 3

Programming

This chapter contains programming instructions for the 12-bit Analog Output Board, and is divided into the following sections:

- Introduction to Programming the 12-bit Analog Output Board
- Control and Status Register Description
- Initialization
- Controlling the Analog Outputs

Introduction to Programming the 12-bit Analog Output Board

Communication with the 12-bit Analog Output Board takes place through 32 contiguous 16-bit register locations which are mapped into the VME short I/O address space. The short I/O address space consists of all locations within the address range from NNNN0000 HEX to NNNNFFFF HEX*. A memory map for the 12-bit Analog Output Board is given in Table 3-1 on page 3-4.

* The value of NNNN depends on the make and model of the controlling CPU.

Control and Status Register Description

The communication register located at relative address 02H is the Control and Status Register (CSR), and contains all of the flags necessary to control and monitor the following board operations:

- Front panel Fail indicator (LED)
- Two's complement or straight binary operation
- Analog voltage outputs on-line/off-line
- Analog current outputs on-line/off-line
- Analog outputs refresh rate
- SCAN HALT

The CSR is 8 bits in length, and is detailed in Table 3-2 on page 3-5. The function of each CSR bit is described in detail subsequently in the associated programming discussions.

Initialization

When SYSTEM RESET is applied to the board, all bits of the Control Register are cleared to the LOW state "zero".

Table 3-1: 12-bit Analog Output Board Memory Map

Relative HEX	Address DEC	Register Name	Access Mode
00	00	BOARD IDENTIFICATION	READ (16XX HEX)
02	02	CSR	READ/WR
04 to 1E	04 to 30	(RESERVED)	–
20	32	ANALOG OUTPUT CHANNEL 00	READ/WRITE
22	34	ANALOG OUTPUT CHANNEL 01	READ/WRITE
24	36	ANALOG OUTPUT CHANNEL 02	READ/WRITE
26	38	ANALOG OUTPUT CHANNEL 03	READ/WRITE
28	40	ANALOG OUTPUT CHANNEL 04	READ/WRITE
2A	42	ANALOG OUTPUT CHANNEL 05	READ/WRITE
2C	44	ANALOG OUTPUT CHANNEL 06	READ/WRITE
2E	46	ANALOG OUTPUT CHANNEL 07	READ/WRITE
30	48	ANALOG OUTPUT CHANNEL 08	READ/WRITE
32	50	ANALOG OUTPUT CHANNEL 09	READ/WRITE
34	52	ANALOG OUTPUT CHANNEL 10	READ/WRITE
36	54	ANALOG OUTPUT CHANNEL 11	READ/WRITE
38	56	ANALOG OUTPUT CHANNEL 12	READ/WRITE
3A	58	ANALOG OUTPUT CHANNEL 13	READ/WRITE
3C	60	ANALOG OUTPUT CHANNEL 14	READ/WRITE
3E	62	ANALOG OUTPUT CHANNEL 15	READ/WRITE

* Register address is the sum of the relative address and the board address.

Table 3-2: Control and Status Register (CSR) Functions

Control Register Data Format							
MSB				LSB			
Bit D15	Bit D14	Bit D13	Bit D12	Bit D11	Bit D10	Bit D09	Bit D08
Reserved	Fail LED L	Reserved	Two's COMPL L	V OUTPUT on H	CURRENT on H	SCAN HALT	FAST REFRESH H
Bit D07	Bit D06	Bit D05	Bit D04	Bit D03	Bit D02	Bit D01	Bit D00
Reserved							

Control and Status Register Bit Definitions

- Bit D15:** **Reserved** – Write a letter “zero” to this bit.
- Bit D14:** **Fail LED L** – The Fail LED is OFF if this bit is set to “one”, and is ON if the bit is “zero”.
- Bit D13:** **Reserved** – Write a letter “zero” to this bit.
- Bit D12:** **Two’s COMPL L** – DAC coding format is straight binary if D12 is “one” (HIGH), two’s complement if D12 is “zero” (LOW).
- Bit D11:** **V OUTPUT on H** – (Also called “ANALOG VOLTAGE OUTPUT ON-LINE.”) If D11 is set to “one”, the current outputs are enabled.
- Bit D10:** **CURRENT on H** – (Also called “ANALOG CURRENT OUTPUT ON-LINE.”) If D10 is set to “one”, the current outputs are enabled.

Note

D11 and D10 must both be set for the current output to operate correctly.

- Bit D09:** **SCAN HALT** – When D9 is set to “one”, the refresh control logic sequencer is halted.
- Bit D08:** **FAST REFRESH H** – The nominal analog output refresh interval is 1.7 ms if D8 is “zero”, 0.6 ms if D8 is “one”.
- Bit D07 through D00:** **Reserved** – Write a letter “zero” to these bits.

Controlling the Analog Outputs

The 16 analog output channels appear to the controlling processor as 16 consecutive 12-bit words in the address space assigned to the 12-bit Analog Output Board. The communication register map shown in Table 3-1 on page 3-4 lists the board-relative address of each output channel. Each analog output register supports both *read* and *write* operations, eliminating the need for corresponding "shadow" latches in the processor Random Access Memory (RAM) space.

Writing to Outputs

Digital codes are recognized in the Analog Output Registers as right-justified 12-bit binary data. Data written to the upper four Most Significant Bits (MSBs) (D12 to D15) will be ignored, and will not be retained for read back. Each output will respond to a new code within 1.7 ms after the code is written to the output register (0.6 ms in FAST REFRESH MODE).

The Digital-to-Analog (D/A) coding conventions used by the D/A Converter (DAC) are shown below. A few examples are given in Table 3-3 on page 3-7.

$$\text{OUTPUT (straight binary)} = (\text{DAC_INPUT}/4096) \times (\text{MAX_OUT} - \text{MIN_OUT}) + \text{MIN_OUT}$$

where DAC_INPUT ranges from 0 to 4095 decimal (0 to FFF HEX), MAX_OUT is the DAC output with FFF HEX as the input and MIN_OUT is the DAC output with "000" as the input.

$$\text{OUTPUT (two's complement)} = (\text{MAX_OUT} - \text{MIN_OUT})/2 + (\text{DAC_INPUT}/4096) \times (\text{MAX_OUT} - \text{MIN_OUT})$$

where DAC_INPUT ranges from -2048 to 2047 decimal (800 to 7FF HEX), MAX_OUT is the DAC output with 7FF HEX as the input and MIN_OUT is the DAC output with 800 HEX as the input.

FAST REFRESH

Setting the FAST REFRESH control bit (Table 3-2 on page 3-5) HIGH will reduce the analog output REFRESH time from the default value of 1.7 ms to 0.6 ms. As each channel is refreshed, there exists associated transient noise which is injected onto the specified output channel. Operating in "FAST REFRESH" mode will increase the rate of these transients. For this reason two refresh rates are available even though this high frequency noise is negligible and will be virtually eliminated when a cable is connected to P3.

Table 3-3: DAC Data Format and Coding

DAC Data Format							
Bit D15	Bit D14	Bit D13	Bit D12	Bit D11	Bit D10	Bit D09	Bit D08
X	X	X	X	D	D	D	D

Bit D07	Bit D06	Bit D05	Bit D04	Bit D03	Bit D02	Bit D01	Bit D00
D	D	D	D	D	D	D	D

DAC Coding							
Unipolar Ranges				Straight Binary			
Output	0 to +10 V	0 to +5 V		D15	D14	D13	D0
+FS LSB	+9.9975 V	+4.9988 V		XXXX	1111	1111	1111
+1/2 FS	+5.0000 V	+2.5000 V		XXXX	1000	0000	0000
+1 LSB	+0.0024 V	+0.0012 V		XXXX	0000	0000	0001
Bipolar Ranges				Offset Binary			
Output	±10 V	±5 V	±2.5 V	D15	D14	D13	D0
+FS LSB	+9.9951 V	+4.9976 V	+2.4988 V	XXXX	1111	1111	1111
+1/2 FS	+5.0000 V	+2.5000 V	+1.2500 V	XXXX	1100	0000	0000
+1 LSB	+0.0049 V	+0.0024 V	+0.0012 V	XXXX	1000	0000	0001
ZERO	0.0000 V	0.0000 V	0.0000 V	XXXX	1000	0000	0000
-FS+1 LSB	-9.9951 V	-4.9976 V	-2.4988 V	XXXX	0000	0000	0001
-FS	-10.0000 V	-5.0000 V	-2.5000 V	XXXX	0000	0000	0000
Bipolar Ranges				Two's Complement			
Output	±10 V	±5 V	±2.5 V	D15	D14	D13	D0
+FS LSB	+9.9951 V	+4.9976 V	+2.4988 V	XXXX	1111	1111	1111
+1/2 FS	+5.0000 V	+2.5000 V	+1.2500 V	XXXX	0100	0000	0000
+1 LSB	+0.0049 V	+0.0024 V	+0.0012 V	XXXX	0000	0000	0001
ZERO	0.0000 V	0.0000 V	0.0000 V	XXXX	0000	0000	0000
-FS+1 LSB	-9.9951 V	-4.9976 V	-2.4988 V	XXXX	1000	0000	0001
-FS	-10.0000 V	-5.0000 V	-2.5000 V	XXXX	1000	0000	0000
Current Ranges				Straight Binary			
Output	0 to 20 mA	4 to 20 mA	5 to 25 mA	D15	D14	D13	D0
+FS LSB	19.9951 mA	19.9961 mA	24.9951 mA	XXXX	1111	1111	1111
+1/2 FS	10.0000 mA	12.0000 mA	15.0000 mA	XXXX	1000	0000	0000
+1 LSB	0.0049 mA	4.0039 mA	5.0049 mA	XXXX	0000	0000	0001
ZERO	0.0000 mA	4.0000 mA	5.0000 mA	XXXX	0000	0000	0000

Off-Line Operation

Setting the V OUTPUT ON H bit enables all channels configured for voltage output. It must be set along with the CURRENT ON H bit to enable the channels configured for current output. See chapter 2 for configuration information. Voltage output channels are in a high-impedance state when they are disabled.

Setting the CURRENT ON H bit (and V OUTPUT ON H) enables all current-output channels. When this bit is low, each channel delivers the minimum for its selected range. For example, any channel set to 4 to 20 mA will source 4 mA. See chapter 2 for range selection information.

Caution

If the 12-bit Analog Output Board is accessed by both user-mode programs and supervisory programs (such as interrupt handlers), they must take care to use the same privilege level. This is because the 12-bit Analog Output Board cannot be jumpered to allow both supervisory and nonprivileged accesses at the same time. One or the other must be selected, but not both.

SCAN HALT

Setting the SCAN HALT bit to one (1) causes the refresh control logic sequencer to halt. Output accuracy cannot be guaranteed with this bit set because the sample-and-hold voltages will begin to droop. Typically, the SCAN HALT bit will not be used during normal operation. Users are advised not to use it (allow it to remain zero (0)).

This 16-channel, 12-bit Analog Output Board is designed to operate in a VMEbus chassis. The following sections describe in detail the theory of operation of the 12-bit Analog Output Board.

This chapter is divided into the following sections:

- Functional Organization
- VMEbus Control Interface
- Analog Outputs
- Built-in-Power Converter
- Board ID Register

Functional Organization

The 12-bit Analog Output Board is divided into the following functional categories. All of the board's functions are discussed in detail in this section.

- VMEbus interface
- Data storage
- DAC and analog distributor
- Analog output buffers and switches
- Voltage-to-current converters
- Analog outputs refresh logic
- Power converter

VMEbus Control Interface

The 12-bit Analog Output Board communications registers are memory mapped as 32 (decimal) 16-bit words. The registers are contiguous, and may be user located on any 64-byte boundary within the short I/O address space of the VMEbus. The board can be user-configured to respond to either short supervisory or nonprivileged bus communications.

During each *read* or *write* operation, all VMEbus control signals are ignored unless the board selection comparator detects a match between the on-board selection jumpers shown in Figure 4-1 on page 4-4 and the address and address-modifier lines from the backplane. The appropriate board response occurs if a valid match is detected, after which the open-collector DTACK interface signal is asserted (driven LOW). Subsequent removal of the Central Processing Unit (CPU) *read* or *write* command causes the board-generated DTACK signal to return to the OFF state.

After board selection has occurred, three groups of VMEbus signals control communications with the board, they are as follows:

- Data bus lines D00 to D15
- Address lines A01, A02, A03, A04, A05
- Bus control signals:
 - (1) WRITE
 - (2) DS0*, DS1*
 - (3) SYS CLK
 - (4) SYS RESET*

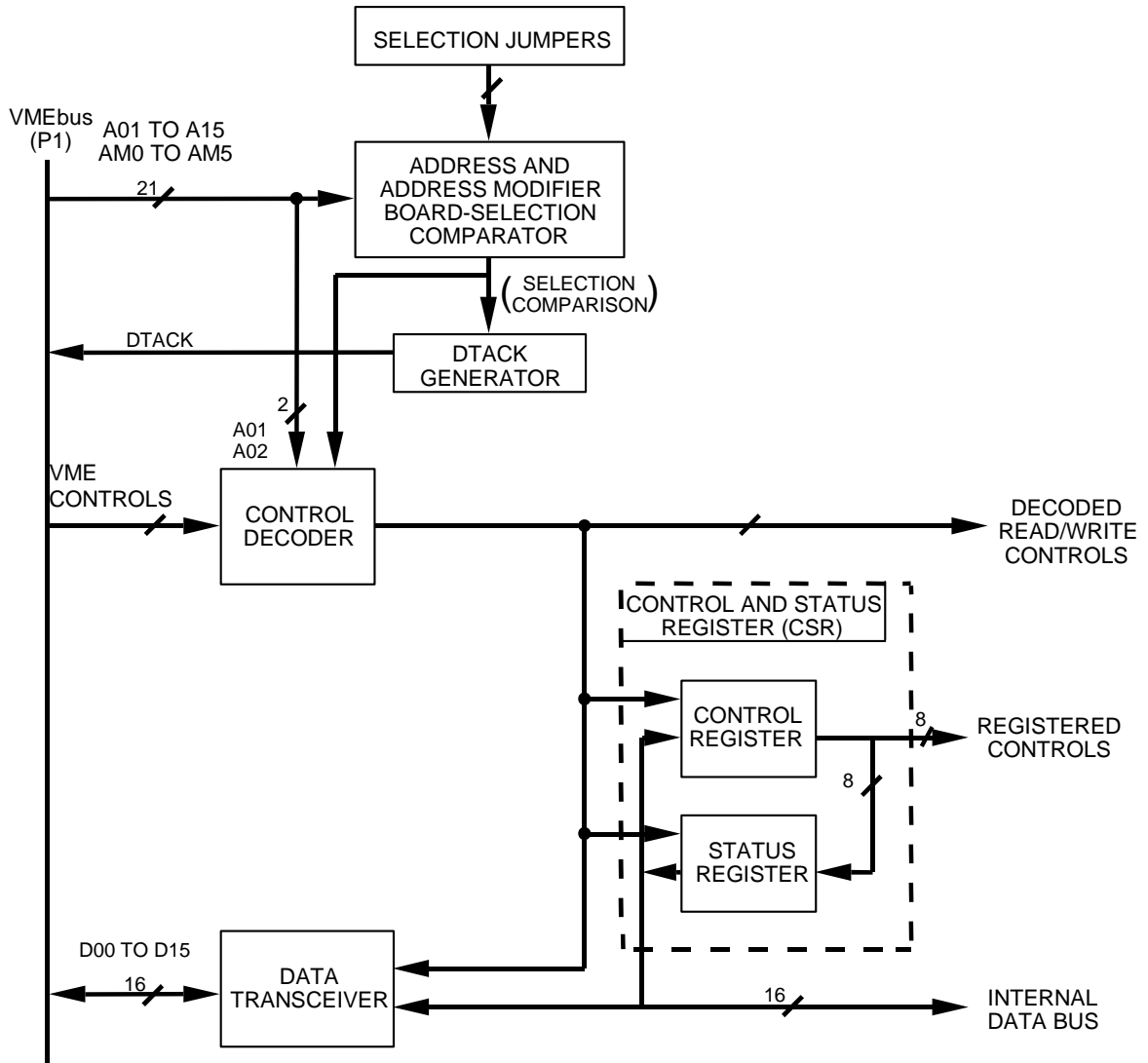
Data bus lines are bi-directional and move data to or from the board through a 16-bit data transceiver in response to control signals from the control decoder. The data transceiver serves as a buffer for the internal data bus which interconnects all data devices on the board.

Address lines A01 through A05 map the 32 communication registers onto a 64-byte range within the VME address space (chapter 3). The control signals determine whether data is to be moved to the board (*write*) or from the board (*read*), provide the necessary data strobes (DS0, DS1), and supply a 16 MHz clock (SYS CLK) for use by on-board timers. A SYS RESET input resets all timers and flags.

Static controls are latched into the Control and Status Register (CSR) and are used primarily to establish the operational mode of the board. The CSR is a *read/write* register. The *WRITE* signal determines whether the CSR is being written to (control), or read from (status).

Each of the 16 analog output channels is controlled by writing 12-bit right-justified data into a dedicated 16-bit *read/write* register. The 16 analog output control registers constitute the VME port of a 16-word dual port memory. The other memory port is controlled by the analog output refresh logic.

Figure 4-1: VMEbus Control Signals and Interface Logic



Analog Outputs

Sixteen analog outputs are available at the P3 connector. The analog outputs are updated (refreshed) periodically from dual port memory by the REFRESH control logic, as illustrated in Figure 4-2 on page 4-6. Each output receives an update once every 1.7 ms in the default refresh mode. A program controlled FAST REFRESH control bit can be used to reduce the refresh cycle time to approximately 0.6 ms, thereby raising the maximum output sampling rate from 588 Hz to 1.6 kHz.

Digital-to-Analog Converter (DAC)

All 16 analog outputs are serviced by a single 12-bit DAC. The DAC is controlled by the REFRESH control logic, which periodically transfers data from the dual port memory to the DAC, and simultaneously connects the DAC to the appropriate section of the analog distributor. Analog output data in the dual port memory is placed there through the VME port by the controlling processor.

Analog Distributor

The analog distributor consists of the following elements:

- One of 16 decoder
- Low charge injection analog demultiplexer
- Sixteen capacitive storage elements

As the DAC is updated with data for each channel in the output REFRESH sequence, the one of 16 decoder receives the same four address lines that are used to select the dual port memory data location. In this manner, the converted analog level is always routed to the distributor section which corresponds to the dual port memory location for the same channel.

After allowing the DAC to settle, the REFRESH logic enables (turns ON) the demultiplexer, and the converted voltage level is transferred to the corresponding storage capacitor. A settling interval of approximately 100 μ s is provided by the REFRESH logic, after which the demultiplexer is disabled and the next channel in the REFRESH sequence is accessed.

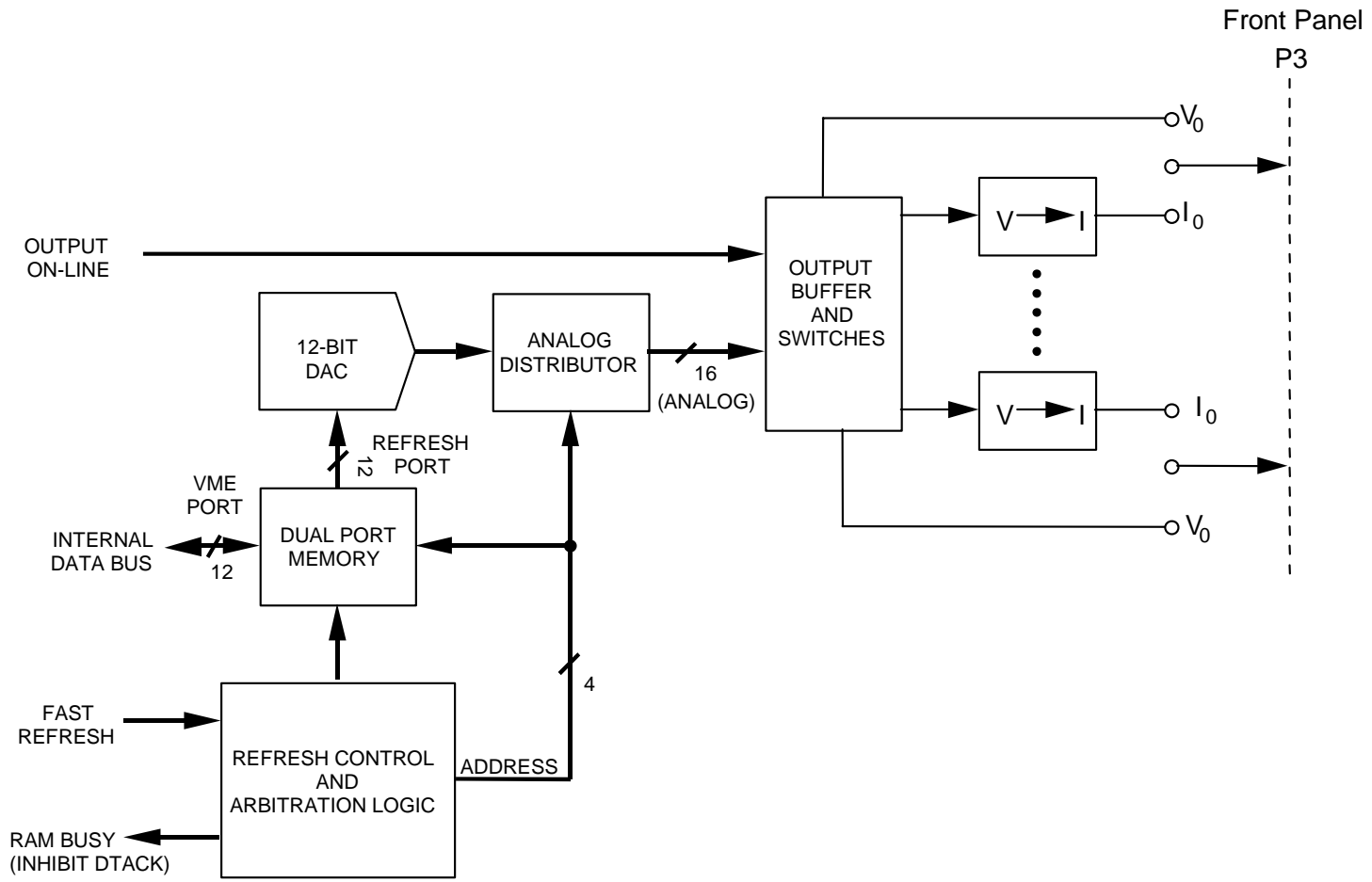


Figure 4-2: Analog Output Circuitry

Output Buffers and Switches

Voltage levels stored by the analog distributor are buffered and then switched to either the P3 connector, or to the voltage-to-current converters. The output buffers are low leakage, precision operational amplifiers which can supply 5 mA of drive current over the full available output voltage range of ± 10 V (at the specified accuracy), and which can withstand sustained short circuits-to-ground without damage.

Output switches permit the analog voltage outputs to be disconnected from P3. To eliminate the effect of switch resistance on output impedance, the inverting (sense) input of each output buffer is switched between the load and line side of the output switch for on-line and off-line operation. Clamping diodes protect the buffers and switches from line transients by preventing voltage excursions beyond the ± 15 V supply rails.

Current outputs are produced by connecting the voltage levels discussed previously in this section to the voltage-to-current conversion circuitry and connecting the current outputs to the P3 connector (both of these connections are made with jumpers as shown in Figure 2-2 on page 2-9). Typically the voltage range is set to 0 to +10 V to produce 4 to 20 mA, 0 to 20 mA or 5 to 25 mA. A voltage range of 0 to +5 V can be selected to produce 4 to 12 mA, 0 to 10 mA or 5 to 15 mA.

Data RAM and Refresh Control

The dual port memory which services the analog outputs is organized as a 12-bit wide, 16-location array, in which each location can be accessed from either of two ports. The random access VME port is used by the VME host to load the analog output digital codes into the memory. The digital codes are then transferred sequentially through the DAC port to the DAC, where they are converted into voltage levels and subsequently distributed to the appropriate analog output channels. The REFRESH logic control sequence is shown in flow diagram form in Figure 4-3 on page 4-10.

Operation of the dual port memory is controlled by the REFRESH control logic which derives its timing from the 16 MHz system clock. The REFRESH control logic supervises all data transfers between the memory and the DAC, and controls the distribution of analog voltage levels to the analog outputs. (Refer to the preceding sections for specific functions of the REFRESH logic.)

Because the dual port memory must be accessed through both the VME and DAC ports, arbitration logic is employed during the transfer of data to the DAC to ensure that only one port is active at any time.

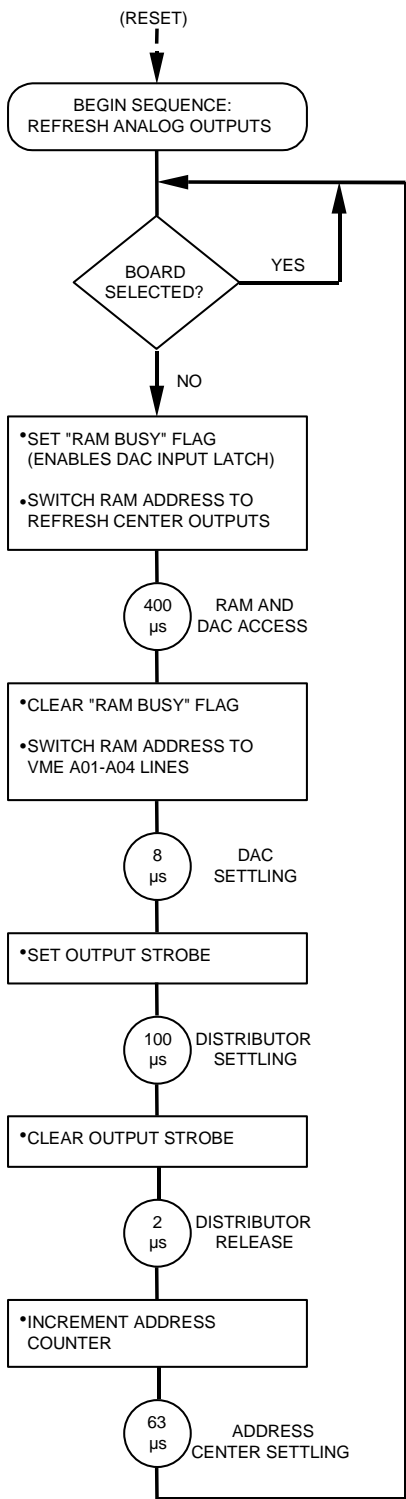
Built-in-Power Converter

Electrical power for the 12-bit Analog Output Board analog network is supplied by the DC-to-DC converters. The converters transform 5 V logic power into regulated and isolated ± 15 VDC power, with a load capacity of approximately 670 mA at +15 V and 330 mA at -15 VDC.

Board ID Register

The first word location of the 12-bit Analog Output Board's memory map is a read-only register. It always reads 16xx (HEX; the last two digits are not specified). Other GE Fanuc products have similar registers which read different constants. This allows general purpose system software to automatically determine which boards have been installed (by reading from a predetermined list of addresses). The configuration software must be able to handle a bus error if it happens to read an empty location.

Figure 4-3: Analog Outputs Refresh Logic; Flow Diagram



Chapter 5

Maintenance

This chapter provides information relative to the care and maintenance of the 12-bit Analog Output Board product.

If the product malfunctions, verify the following:

- Software
- System configuration
- Electrical connections
- Jumper or configuration settings
- Boards fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the VMEbus card cage
- Quality of cables and I/O connections

User level repairs are not recommended. Contact your authorized GE Fanuc distributor for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**