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# GE Fanuc Automation

*Programmable Control Products*

## *IC697VDQ120*
## *Digital Output, 64-Point, 24VDC Board*

***User's Manual***

*GFK-2066* *514-000442-000 A* *December 2001*

# *Warnings, Cautions, and Notes as Used in this Publication*

## Warning

**Warning notices are used in this publication to emphasize that hazardous voltages, currents, temperatures, or other conditions that could cause personal injury exist in this equipment or may be associated with its use.**

**In situations where inattention could cause either personal injury or damage to equipment, a Warning notice is used.**

## Caution

**Caution notices are used where equipment might be damaged if care is not taken.**

## Note

Notes merely call attention to information that is especially significant to understanding and operating the equipment.

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| CIMSTAR | Modelmaster | Series 90 | VersaPro |
| Field Control | Motion Mate | Series Five | VuMaster |
| GEnet | ProLoop | Series One | Workmaster |

# *Contents*

# Chapter 1 Introduction, Description, and Specifications

This manual describes the installation and operation of the IC697VDQ120 Digital Output, 64-point, 24VDC Board.

## Reference Material and Other GE Fanuc Manuals

For a detailed explanation of the VMEbus and its characteristics, "The VMEbus Specification" is available from:

VITA
VMEbus International Trade Association
7825 East Gelding Dr., No. 104
Scottsdale, AZ 85260
(480) 951-8866
FAX: (480) 951-0720
Internet: www.vita.com

The following Application Guide is available from GE Fanuc to assist in the selection, specification, and implementation of systems based upon GE Fanuc's products:

| | |
|---|---|
| Connector and I/O Cable Application Guide (catalog number GFK-2085) | Describes I/O connections that can be used with GE Fanuc's VMEbus products. Includes connector compatibility information and examples. |

# General Description

The Digital Output Board is capable of delivering 64 channels of high current output. These outputs can be current sourcing or current sinking. The Digital Output Board is designed with a breakdown voltage of 35 V minimum. A unique feature of the Digital Output Board is the Built-in-Test (BIT) logic, which allows the user, under software control, to verify the operation of each channel.

A brief overview of the Digital Output Board's features includes:

- 64 bits of high current outputs.
- Outputs may be current sourcing/High-Z or current source/sinks.
- Output transient protected.
- High-breakdown voltage (35 V minimum).
- Tri-state outputs.
- Built-in-Test logic for fault isolation.
- High reliability DIN type output connectors.
- 8-, 16-, or 32-bit transfers.
- Double Eurocard form factor.
- ±3.5 A peak output current (100 msec, 10 percent duty cycle).
- 500 mA continuous current (fan cooled).
- Thermal shutdown protection.
- Front panel software controlled Failed LED for Built-in-Test.
- Separate user configurable address jumpers for the Control and Status Register (CSR) and the Data Registers allow for contiguous data addressing when more than one I/O board is used in a VMEbus system.

# *Functional Description*

The Digital Output Board is designed with common programming features such that subsystems may be configured with contiguous I/O addresses to conserve memory. Each Digital Output board is designed with two sets of board address switches or jumpers to provide an efficient memory address map for CSR and I/O addresses. CSR addresses may be set such that all CSRs among a variety of boards in the system may be mapped into contiguous memory locations separate from the I/O data addresses.

The Digital Output Board features a front panel Fail LED that is illuminated at power-up or after a system reset. The Fail LED may be extinguished under program control upon successful completion of board level diagnostics. Specific hardware has been designed into the Digital Output Board to support the Built-in-Test functions. The Digital Output Board also supports both off-line and on-line fault detection and isolation.

# Safety Summary

**The following general safety precautions must be observed during all phases of this operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product. GE Fanuc assumes no liability for the customer's failure to comply with these requirements.**

## Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

## Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

## Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

## Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

## Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to GE Fanuc for service and repair to ensure that safety features are maintained.

# Chapter 2 Configuration and Installation

This chapter, divided into the following sections, provides configuration and installation instructions for the Digital Output Board:

- Physical Installation
- Jumper Locations
- Suppressor Diode Connections
- Address Modifiers
- Address Selection Jumpers
- I/O Cable and Front Panel Connector Configuration
- Jumper Functions

**Caution**

**Some of the components assembled on GE Fanuc's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. Unused boards should be stored in the same protective boxes as shipped. When the board is to be laid on a bench for configuring, ect., it is suggested that conductive material be inserted under the board to provide a conductive shunt.**

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged printed circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to GE Fanuc together with a request for advice concerning the disposition of the damaged item(s).

# Physical Installation

**Caution**

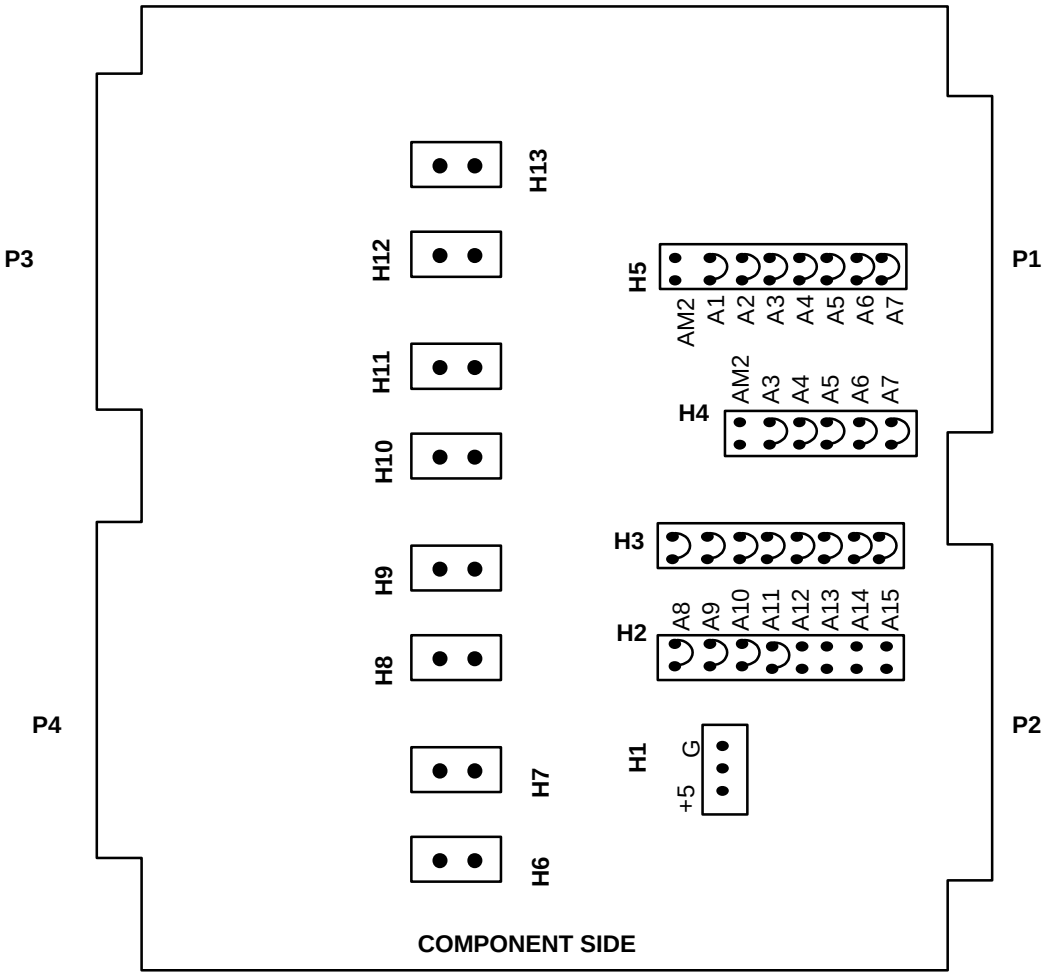
**Do not install or remove boards while power is applied.**

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

# *Jumper Locations*

The physical positions of the jumpers described in this section are shown in Figure 2-1.

Figure 2-1: Jumper Locations Showing Factory Configuration



# Suppressor Diode Connections

The output drivers of the Digital Output Board have built-in suppressor diodes for driving inductive loads. Thus, the user does not need to add diodes to his circuitry. A typical output driver stage is shown in Figure 2-2 on page 2-8.

# *Address Modifiers*

The Digital Output Board is configured at the factory to respond to short supervisory I/O access. This configuration can be changed to short nonprivileged I/O access by installing jumpers in position AM2 of the headers H4 and H5. H4 is for the Output Registers, and H5 is for the CSR.

# Address Selection Jumpers

The Digital Output Board is designed with two banks of address select jumpers that specify the beginning board address for the Data Registers and the address of the CSR. The address selection jumpers are shown in Figures 2-3 on page 2-9 and Figure 2-4 on page 2-10. These jumpers are used like an address switch, installing a jumper places the corresponding address bit to a logic "zero". If the jumper is removed, then the corresponding address bit will be a logic "one". The Digital Output Board is factory configured to respond to 0000 HEX for Data Registers and to F000 HEX for the CSR.

# *I/O Cable and Front Panel Connector Configuration*

The output connectors (P3 and P4) on the Digital Output Board are 64-pin DIN standard and were selected by GE Fanuc because of their high quality. Although these connectors are generally used with flat-ribbon cables, a variety of cables and mating connectors are available for most user requirements. The user should refer to GE Fanuc's Connector and I/O Cable Application Guide (GE Fanuc Document No. GFK-2085) for additional information concerning the variety of possible cabling and connector types available.

Figure 2-2: Typical Output Driver Stage

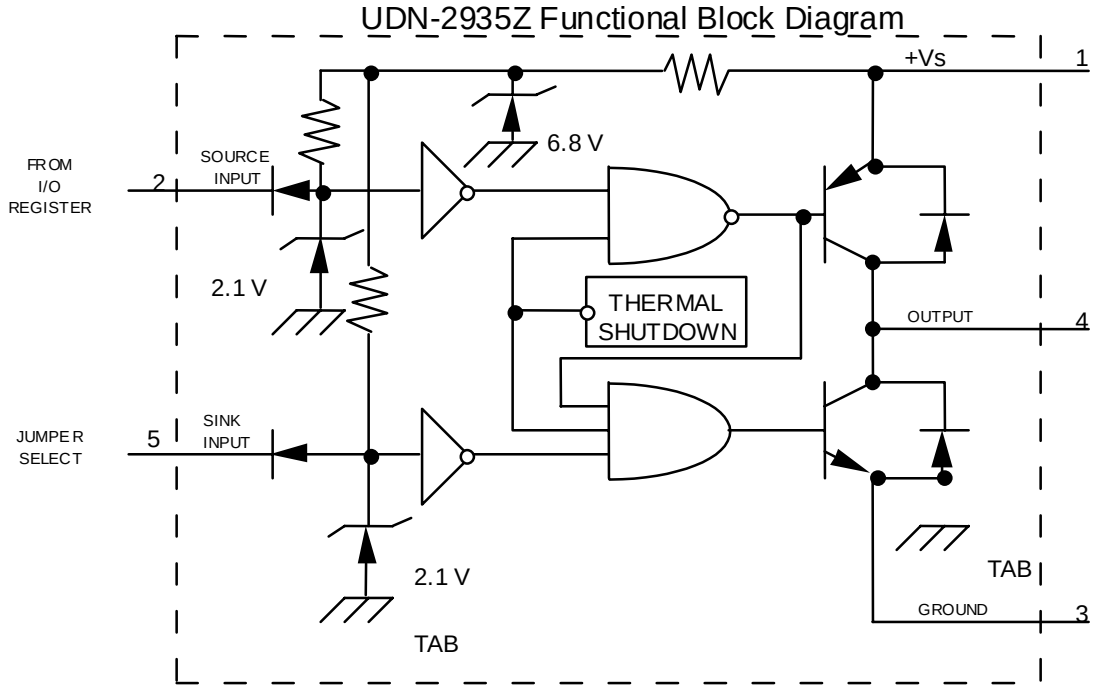
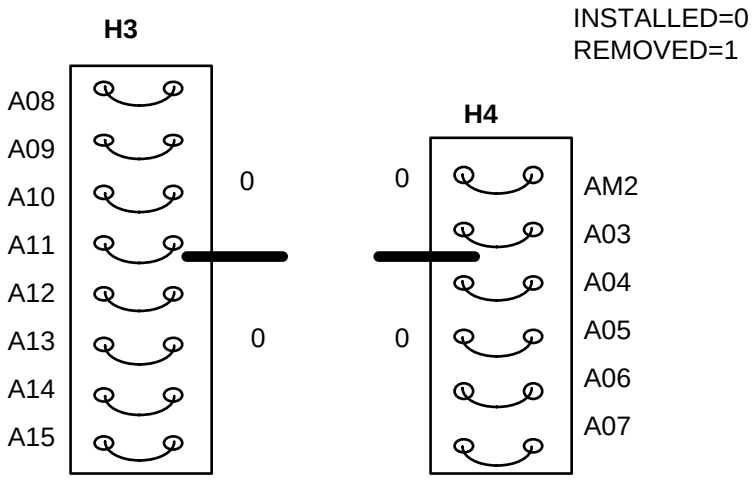



**Table 2-1: Logic Truth Table**

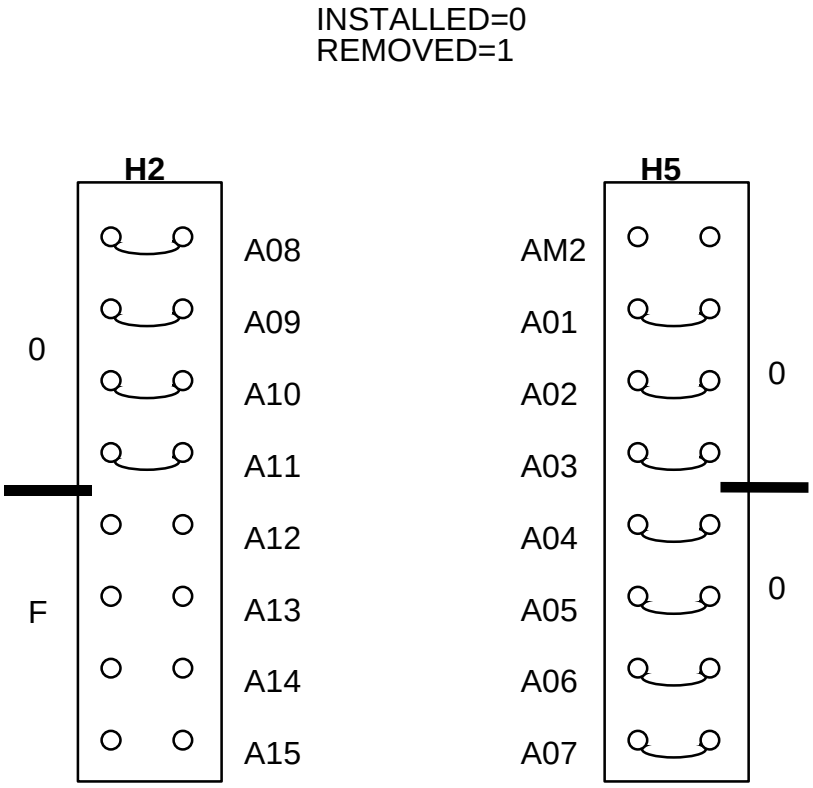
| Data Register Input, $V_2$ | Jumper Select Input, $V_5$ | Output $V_4$ |
|---|---|---|
| Low | Low | High |
| Low | High | High |
| High | Low | Low |
| High | High | High Z |

Figure 2-3: Data Register Base Address Select Jumpers




THE EXAMPLE SHOWN IS FOR BASE ADDRESS OF 0000 HEXADECIMAL

Figure 2-4: CSR Base Address Select Jumpers




THE EXAMPLE SHOWN IS FOR BASE ADDRESS OF F000 (Hexadecimal)

Figure 2-5: P3/P4 Connector – Pin Configuration

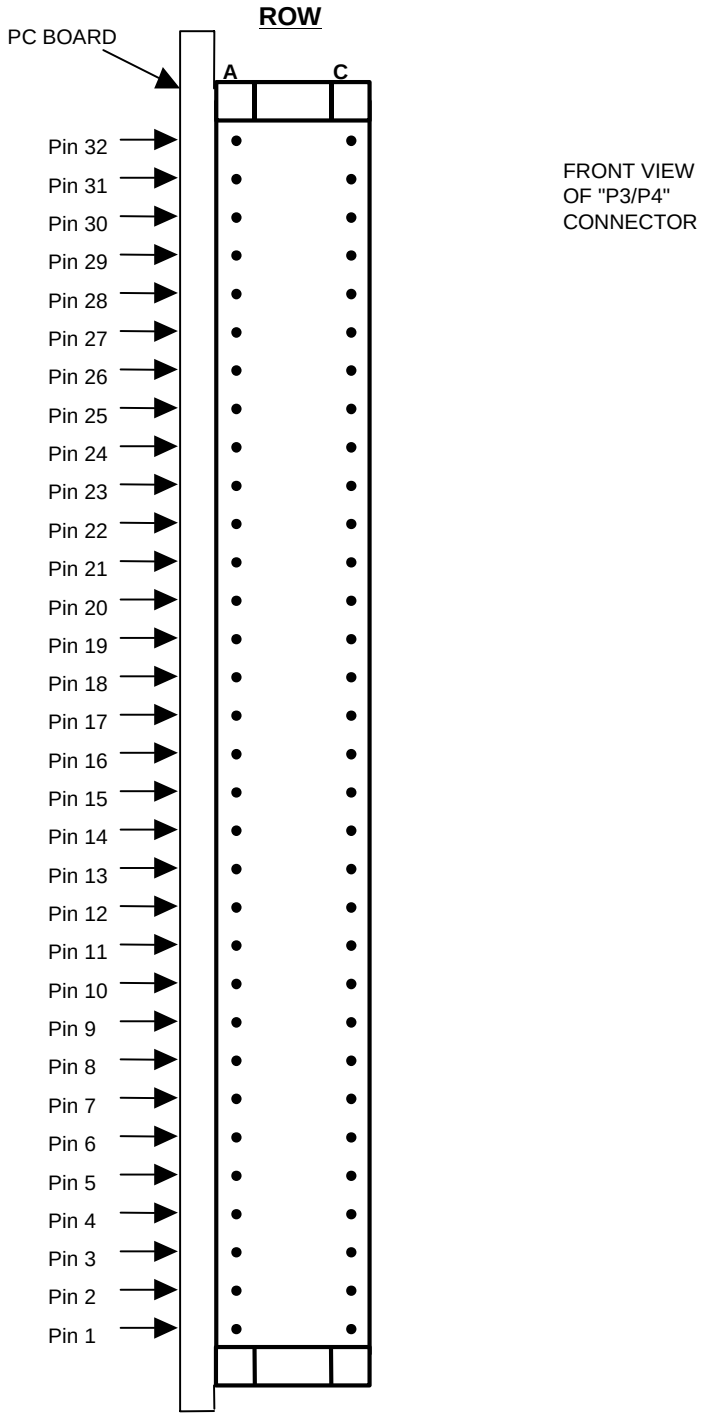


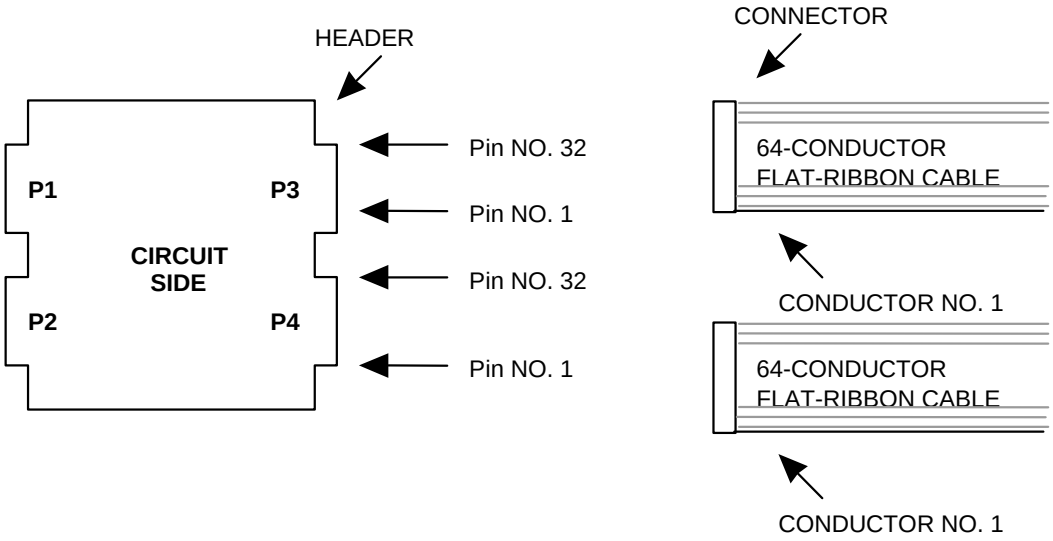
**Table 2-2: Connector P4 Pin/Channel Assignments**

| Pin Number | Row A (Signal Usage) | Row C (Signal Usage) |
|---|---|---|
| 1 | CH00/01 VI | CH00 VO |
| 2 | GND | CH01 VO |
| 3 | CH02/03 VI | CH02 VO |
| 4 | GND | CH03 VO |
| 5 | CH04/05 VI | CH04 VO |
| 6 | GND | CH05 VO |
| 7 | CH06/07 VI | CH06 VO |
| 8 | GND | CH07 VO |
| 9 | CH08/09 VI | CH08 VO |
| 10 | GND | CH09 VO |
| 11 | CH10/11 VI | CH10 VO |
| 12 | GND | CH11 VO |
| 13 | CH12/13 VI | CH12 VO |
| 14 | GND | CH13 VO |
| 15 | CH14/15 VI | CH14 VO |
| 16 | GND | CH15 VO |
| 17 | CH16/17 VI | CH16 VO |
| 18 | GND | CH17 VO |
| 19 | CH18/19 VI | CH18 VO |
| 20 | GND | CH19 VO |
| 21 | CH20/21 VI | CH20 VO |
| 22 | GND | CH21 VO |
| 23 | CH22/23 VI | CH22 VO |
| 24 | GND | CH23 VO |
| 25 | CH24/25 VI | CH24 VO |
| 26 | GND | CH25 VO |
| 27 | CH26/27 VI | CH26 VO |
| 28 | GND | CH27 VO |
| 29 | CH28/29 VI | CH28 VO |
| 30 | GND | CH29 VO |
| 31 | CH30/31 VI | CH30 VO |
| 32 | GND | CH31 VO |

**Table 2-3: Connector P3 Pin/Channel Assignments**

| Pin Number | Row A (Signal Usage) | Row C (Signal Usage) |
|---|---|---|
| 1 | CH32/33 VI | CH32 VO |
| 2 | GND | CH33 VO |
| 3 | CH34/35 VI | CH34 VO |
| 4 | GND | CH35 VO |
| 5 | CH36/37 VI | CH36 VO |
| 6 | GND | CH37 VO |
| 7 | CH38/39 VI | CH38 VO |
| 8 | GND | CH39 VO |
| 9 | CH40/41 VI | CH40 VO |
| 10 | GND | CH41 VO |
| 11 | CH42/43 VI | CH42 VO |
| 12 | GND | CH43 VO |
| 13 | CH44/45 VI | CH44 VO |
| 14 | GND | CH45 VO |
| 15 | CH46/47 VI | CH46 VO |
| 16 | GND | CH47 VO |
| 17 | CH48/49 VI | CH48 VO |
| 18 | GND | CH49 VO |
| 19 | CH50/51 VI | CH50 VO |
| 20 | GND | CH51 VO |
| 21 | CH52/53 VI | CH52 VO |
| 22 | GND | CH53 VO |
| 23 | CH54/55 VI | CH54 VO |
| 24 | GND | CH55 VO |
| 25 | CH56/57 VI | CH56 VO |
| 26 | GND | CH57 VO |
| 27 | CH58/59 VI | CH58 VO |
| 28 | GND | CH59 VO |
| 29 | CH60/61 VI | CH60 VO |
| 30 | GND | CH61 VO |
| 31 | CH62/63 VI | CH62 VO |
| 32 | GND | CH63 VO |

Figure 2-6: Cable Connector Configuration




Output connector pin configurations for P3 and P4 are shown in Figure 2-5 on page 2-11. Connector pin assignments for the 64 output channels are shown in Table 2-2 on page 2-12 and Table 2-3 on page 2-13. The signals on row A of the connectors are used by two output drivers (as stated in the signal name). These power lines should be returned directly to the power source of the external circuitry. This is to help prevent excessive current from flowing in the backplane. A compatible flat-ribbon cable connector is Panduit No. 120-964-435E. A compatible strain relief is Panduit No. 100-000-032. Cable connector configuration is shown in Figure 2-6 above.

**Caution**

**The user should use the cable ground lines for the external power supply returns. This is required to prevent excessive current from flowing into the VMEbus backplane. Also, the user should remove power before the cables are connected or disconnected (from the board). This will prevent excessive currents from damaging the P3/P4 connector pins.**

# *Jumper Functions*

Jumper H1 is provided to invert the data written to the Control and Status Register (CSR). It is configured at the factory such that the test software writes positive data to the CSR (this board uses positive true data polarity).

Jumpers H6 through H13 are used to select the mode of operation for output drivers. If the jumper is not installed, the output devices operate in the current source mode. With the jumper installed, the associated output drivers will source as well as sink current (depending on output logic level). Please refer to the logic truth table (Table 2-1) on page 2-8 for the logical operation of these devices. This table is based on an impedance to ground.

# Chapter 3 Programming

This chapter contains programming instructions for the Digital Output Board, and is divided into the following sections:

- Register Map
- Register Bit Definitions
- Detailed Programming

# Register Map

The Digital Output Board contains eight 8-bit Output Data Registers and an 8-bit Control and Status Register (CSR). These Output Data Registers allow access to 64 current source/sink output channels and are addressable as two 32-bit longwords, four 16-bit words, or as eight 8-bit bytes. The Output Data Registers also support bi-directional transfers, which is used for data validation or diagnostic testing. The CSR is addressable as a 16-bit word or as two 8-bit bytes. It is a write-only register.

**Table 3-1: Data Registers**

| Relative Address | Mnemonic | Name/Function |
|---|---|---|
| $XXX0 | DR0 | DATA REGISTER 0 |
| $XXX1 | DR1 | DATA REGISTER 1 |
| $XXX2 | DR2 | DATA REGISTER 2 |
| $XXX3 | DR3 | DATA REGISTER 3 |
| $XXX4 | DR4 | DATA REGISTER 4 |
| $XXX5 | DR5 | DATA REGISTER 5 |
| $XXX6 | DR6 | DATA REGISTER 6 |
| $XXX7 | DR7 | DATA REGISTER 7 |

XXX of the address is determined by data register address select jumpers as shown in Chapter 2.

DR0 to DR7 are read/write registers.

**Table 3-2: CSRs**

| Relative Address | Mnemonic | Name/Function |
|---|---|---|
| $YYY0 | CSRU | CSR UPPER BYTE |
| $YYY1 | CSRL | CSR LOWER BYTE |

YYY of the address is determined by CSR address select jumpers as shown in Chapter 2.

The CSR is a write-only register.

# *Register Bit Definitions*

The following tables (Table 3-3 and Table 3-4) will list and define the bits established by the output channels and the registers that contain the bits as used by the Digital Output Board.

**Table 3-3: Output Data Register Bit Definitions**

| **Output Data Register $XXX0 DR0** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 31** | **Bit 30** | **Bit 29** | **Bit 28** | **Bit 27** | **Bit 26** | **Bit 25** | **Bit 24** |
| OD63 | OD62 | OD61 | OD60 | OD59 | OD58 | OD57 | OD56 |

| **Output Data Register $XXX1 DR1** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 23** | **Bit 22** | **Bit 21** | **Bit 20** | **Bit 19** | **Bit 18** | **Bit 17** | **Bit 16** |
| OD55 | OD54 | OD53 | OD52 | OD51 | OD50 | OD49 | OD48 |

| **Output Data Register $XXX2 DR2** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 15** | **Bit 14** | **Bit 13** | **Bit 12** | **Bit 11** | **Bit 10** | **Bit 09** | **Bit 08** |
| OD47 | OD46 | OD45 | OD44 | OD43 | OD42 | OD41 | OD40 |

| **Output Data Register $XXX3 DR3** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 07** | **Bit 06** | **Bit 05** | **Bit 04** | **Bit 03** | **Bit 02** | **Bit 01** | **Bit 00** |
| OD39 | OD38 | OD37 | OD36 | OD35 | OD34 | OD33 | OD32 |

| **Output Data Register $XXX4 DR4** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 23** | **Bit 22** | **Bit 21** | **Bit 20** | **Bit 19** | **Bit 18** | **Bit 17** | **Bit 16** |
| OD31 | OD30 | OD29 | OD28 | OD27 | OD26 | OD25 | OD24 |

| **Output Data Register $XXX5 DR5** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 15** | **Bit 14** | **Bit 13** | **Bit 12** | **Bit 11** | **Bit 10** | **Bit 09** | **Bit 08** |
| OD23 | OD22 | OD21 | OD20 | OD19 | OD18 | OD17 | OD16 |

| **Output Data Register $XXX6 DR6** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 07** | **Bit 06** | **Bit 05** | **Bit 04** | **Bit 03** | **Bit 02** | **Bit 01** | **Bit 00** |
| OD15 | OD14 | OD13 | OD12 | OD11 | OD10 | OD09 | OD08 |

| **Output Data Register $XXX7 DR7** | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 31** | **Bit 30** | **Bit 29** | **Bit 28** | **Bit 27** | **Bit 26** | **Bit 25** | **Bit 24** |
| OD07 | OD06 | OD05 | OD04 | OD03 | OD02 | OD01 | OD00 |

**Table 3-4: CSR Bit Definitions**

| CSR Bit Definition $YYY0 CSRU | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 15** | **Bit 14** | **Bit 13** | **Bit 12** | **Bit 11** | **Bit 10** | **Bit 09** | **Bit 08** |
| Not used | | | | | | | |

| CSR Bit Definition $YYY1 CSRL | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Bit 07** | **Bit 06** | **Bit 05** | **Bit 04** | **Bit 03** | **Bit 02** | **Bit 01** | **Bit 00** |
| TM=1 | FL=1 | Not used | | | | | |

# *Detailed Programming*

## Output Data Transfers

As seen in the register map on page 3-2, DR0 to DR7 corresponds to output channels 63 to 0. By writing to these Data Registers, any output channel can be controlled.

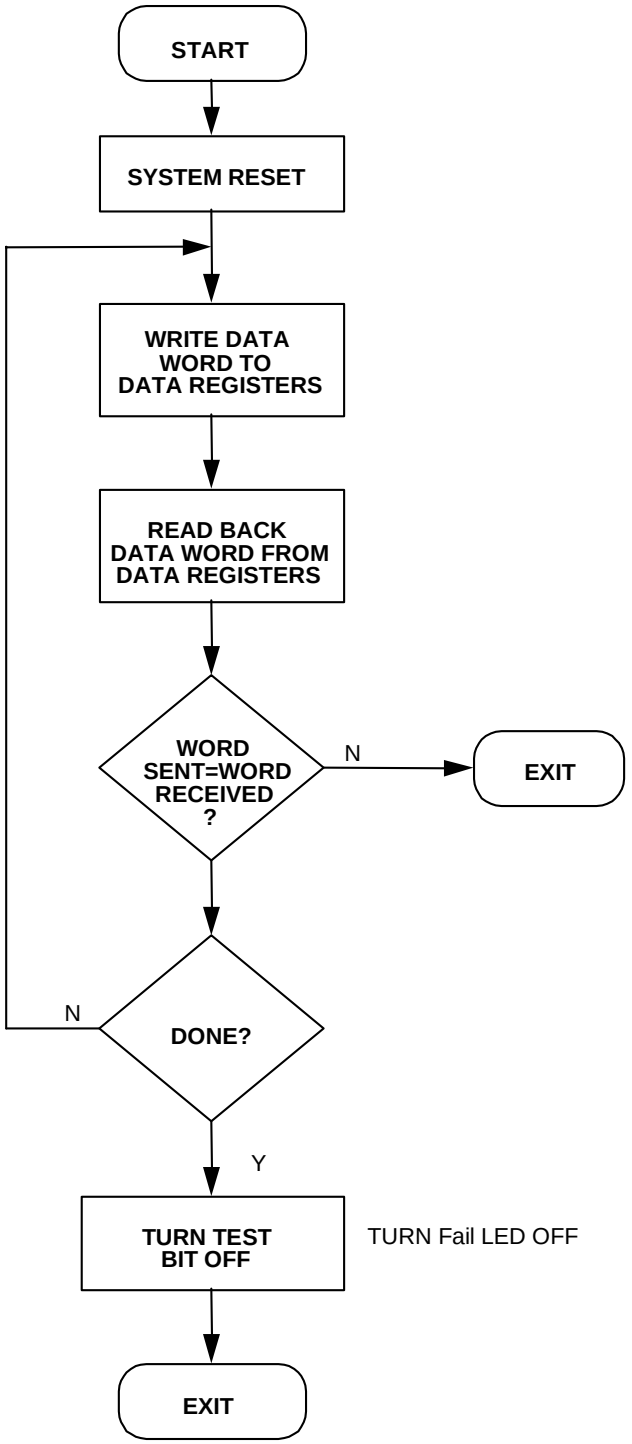
## Built-in-Test

The Built-in-Test features of the Digital Output Board provide the user with the capability of real-time loop-back data verification and off-line diagnostic execution. The off-line Built-in-Test feature is initiated by setting the TM bit in the CSR to a logic "one". Test data may be written to the selected Data Register and read back on a read transfer.

At power-up or after a system reset, the Test Mode and Failed LED bits of the CSR are initialized active (a logic "one"). In Test Mode, the operator may perform diagnostic testing of the board's logic and internal registers. At the end of the diagnostic testing, and assuming the board passes, the operator needs to negate (a logic "zero") the CSR bits used to control Test Mode and the Fail LED. A simplified programming flowchart for Built-in-Test is shown in Figure 3-1 on page 3-6 and Figure 3-2 on page 3-7.

The H1 jumper is set at the factory so that Test Mode is active and the LED is illuminated when a logic "one" is written to the CSR. By altering the H1 jumper (moving from +5 V to ground or from ground to +5 V), the user program can activate Test Mode and illuminate the Fail LED by writing a logic "zero" to the CSR. The configuration of H1 is discussed in greater detail in “Jumper Functions” on page 2-15.

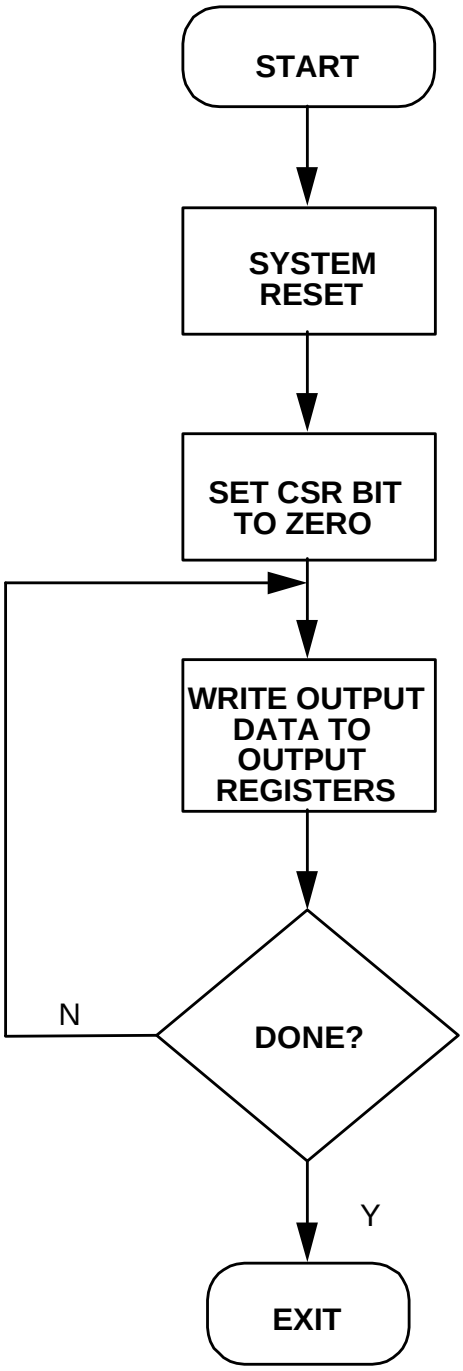
Figure 3-1: Programming Flowchart (Built-in-Test Active)




**Note**

At system reset, the Fail LED is ON and the output drivers are disconnected.

Figure 3-2: Programming Flowchart (Built-in-Test Not Active)




**Note**

At system reset, the output drivers are disconnected and the Fail LED is illuminated.

# Chapter 4 Theory of Operation

This chapter discusses the operation of the Digital Output Board and is divided into the following sections:

- Operational Overview
- Device Addressing
- VMEbus Foundation Logic
- Data Transfers
- Register Control Logic
- Control and Status Register (CSR)
- Built-in-Test
- Octal Registers and Output Drivers

# Operational Overview

The Digital Output Board is designed for a variety of applications such as:

- Relay drivers
- Lamp drivers
- Solenoid drivers
- Hammer drivers
- Stepping motor drivers
- Triac drivers
- LED drivers
- High current, high voltage drivers
- Fiber-optic LED drivers

The design of the Digital Output Board, as shown in the functional block diagram in Figure 4-1 on page 4-4, consists primarily of four sections:

1. Device addressing
2. VMEbus foundation logic
3. Built-in-Test logic
4. Output drivers

The board is designed using eight bi-directional 8-bit registers, a Control and Status Register (CSR), high performance output drivers, typical VMEbus foundation logic, and two device address jumper banks. The two jumper banks provide the user with the capability and flexibility to map I/O registers and CSRs into separate contiguous memory locations.

# Device Addressing

The Digital Output Board is designed to support data transfers in supervisory or nonprivileged short I/O memory space. Jumpers are provided, as shown in Figure 4-2 on page 4-5 (Address Selection Block Diagram), to allow user selection of either I/O access type. These jumpers are called AM2. There is one jumper for the Data Registers and one jumper for the CSR. The Digital Output Board is factory configured (jumpers AM2 not installed) to respond to short supervisory I/O access.

The Digital Output Board is designed with two sets of board select jumpers and decode logic as shown in Figure 4-2 on page 4-5 to provide an efficient memory address map for the CSR and I/O addresses. This feature allows the user to map CSR and I/O addresses into separate contiguous memory locations when configuring subsystems that require more than one board.

Figure 4-1: Digital Output Board Functional Block Diagram

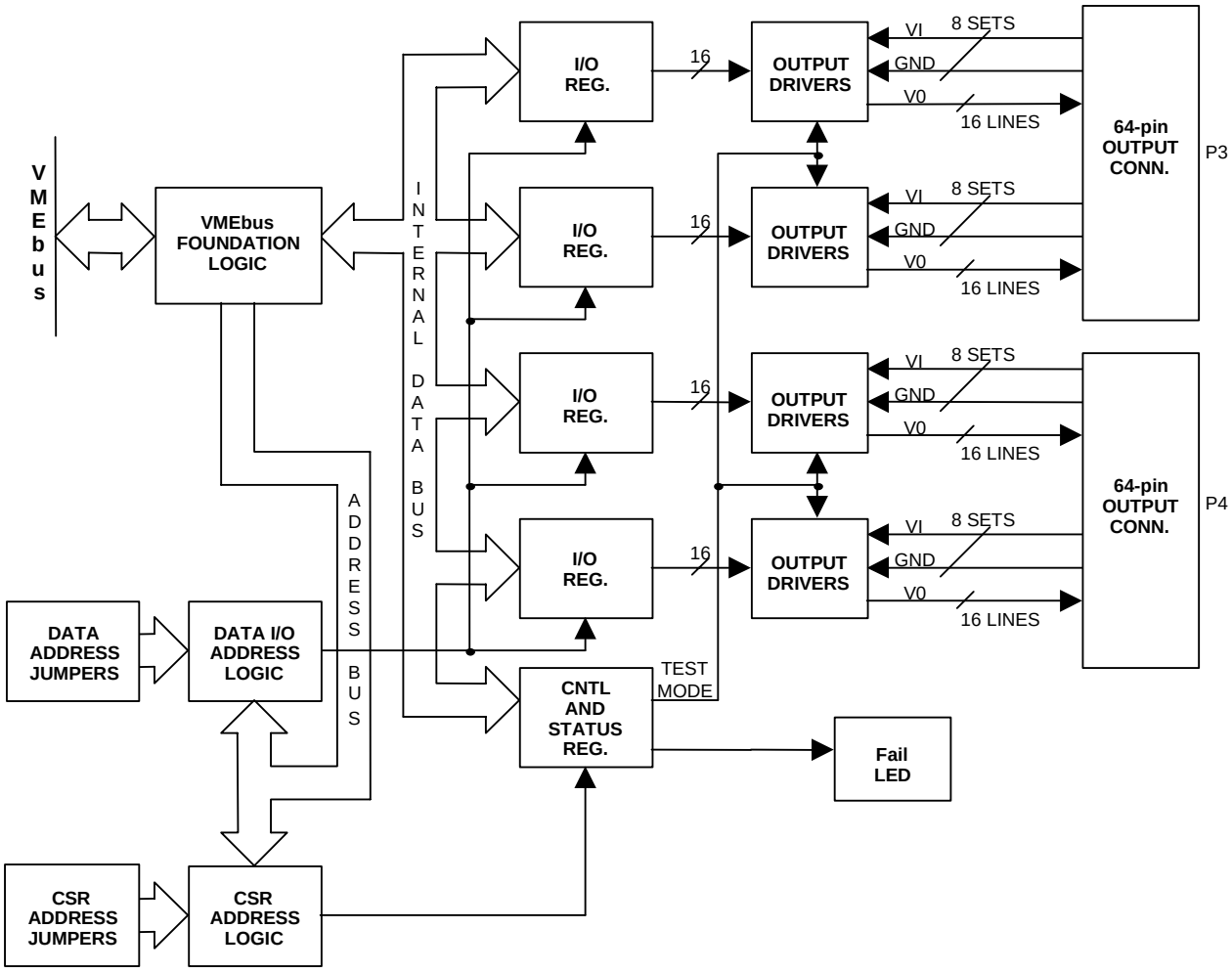
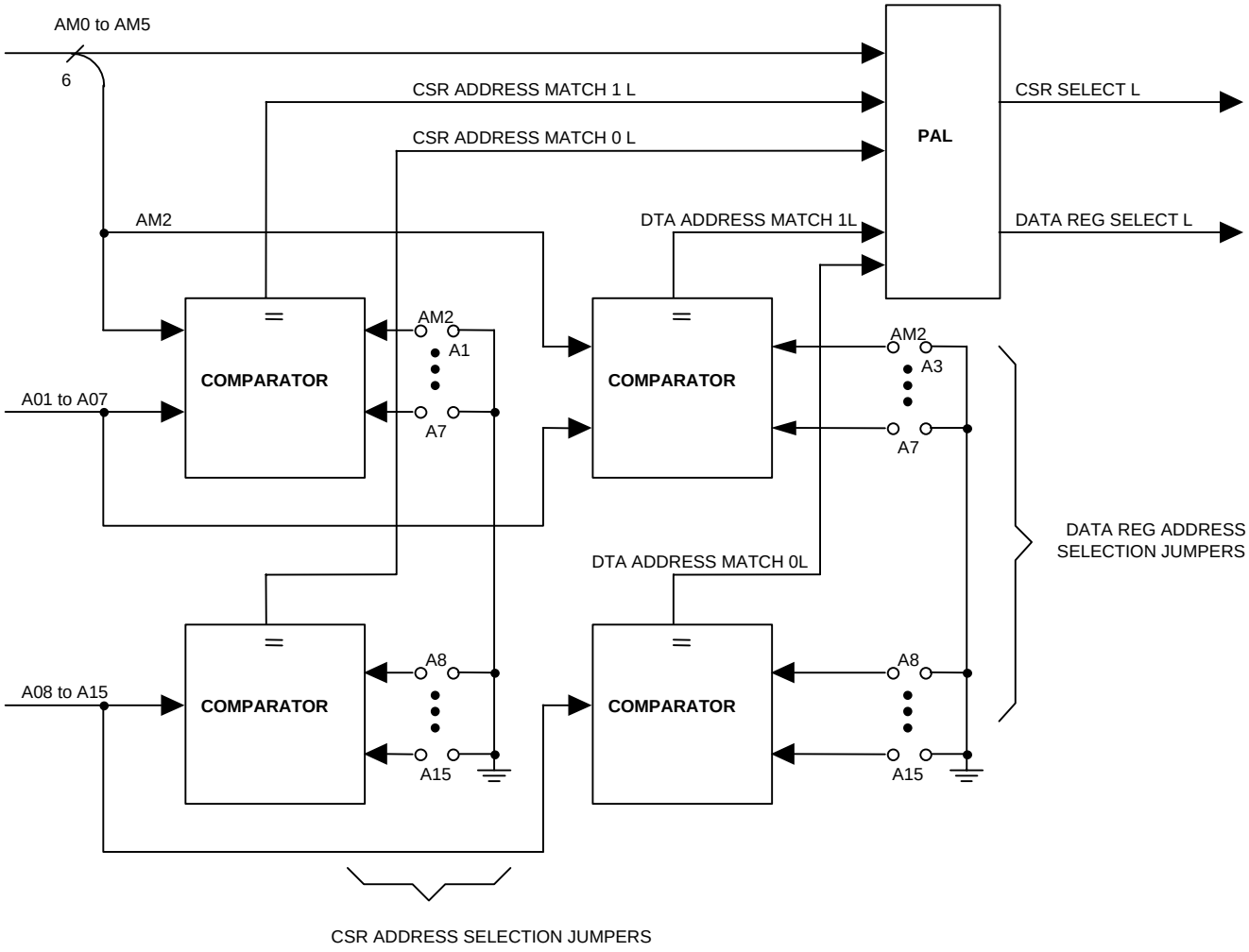


Figure 4-2: Address Selection Block Diagram



# VMEbus Foundation Logic

Typical VMEbus drivers, receivers, and control logic are shown in Figure 4-2 on page 4-5, Figure 4-3 on page 4-11, and Figure 4-4 on page 4-12.

# *Data Transfers*

Data transfer transceivers are shown in Figure 4-5 on page 4-13. The data transceivers are designed to support write and read operations on 8-, 16-, and 32-bit boundaries. Thus, the 64 current source/sink outputs are addressable as two 32-bit longwords, four 16-bit words, or as eight 8-bit bytes.

# Register Control Logic

The register control logic for the Digital Output Board is designed to support write and read operations to and from the eight 8-bit bi-directional dual-port latches and write transfers to a CSR that controls the test mode and front panel LED. The control logic provides the capability to read or write 8, 16, or 32 bits of data. This control logic is implemented in PALs.

# *Control and Status Register (CSR)*

The CSR is a write-only register that controls the Test Mode (TM) bit and the front panel Fail LED as shown in Figure 4-6 on page 4-14. The TM bit disables the output drivers to perform Built-in-Test functions. Both bits of the CSR are initialized active upon system reset or power-up such that the driver outputs are disabled and the front panel LED is illuminated. A jumper H1 is configured such that when writing a logic "one" to bits 6 and 7 of the CSR, the LED is illuminated and the output drivers are off-line.

# Built-in-Test

The Built-in-Test feature of the Digital Output Board is enabled by asserting (setting to a logical "one") the test mode bit in the CSR. As an aid to programming the Digital Output Board, a jumper (H1) is available to the user. This jumper can be used to invert the input data to the CSR of the Digital Output Board. It is used to permit existing software to control the Digital Output Board. If the program used writes "zeros" to the CSR this jumper can be setup to invert this data (since the Digital Output Board uses "ones" in the CSR). This way the H1 jumper can let the user run existing software without modifications.

While in Test Mode, data may be written to any Output Data Register and read back on a following read operation. This way the data written can be compared to the data read and any action necessary can be initiated. While in Test Mode, writing to an output device will have no effect on the field equipment, because the output drivers are disabled during Test Mode operations.

The data loopback circuitry can be used even if TEST MODE is not active. Thus, the Built-in-Test feature of this product provides the user with the capability of performing real-time loopback testing with the output drivers connected to the field equipment.

A front panel Fail LED is provided for quick fault isolation to the board level. The Fail LED is illuminated at power-up or system reset and is extinguished under software control by the user upon successful execution of a user-defined diagnostic program. The board is initialized in the Test Mode at power-up or upon system reset.

Figure 4-3: Control Section Block Diagram

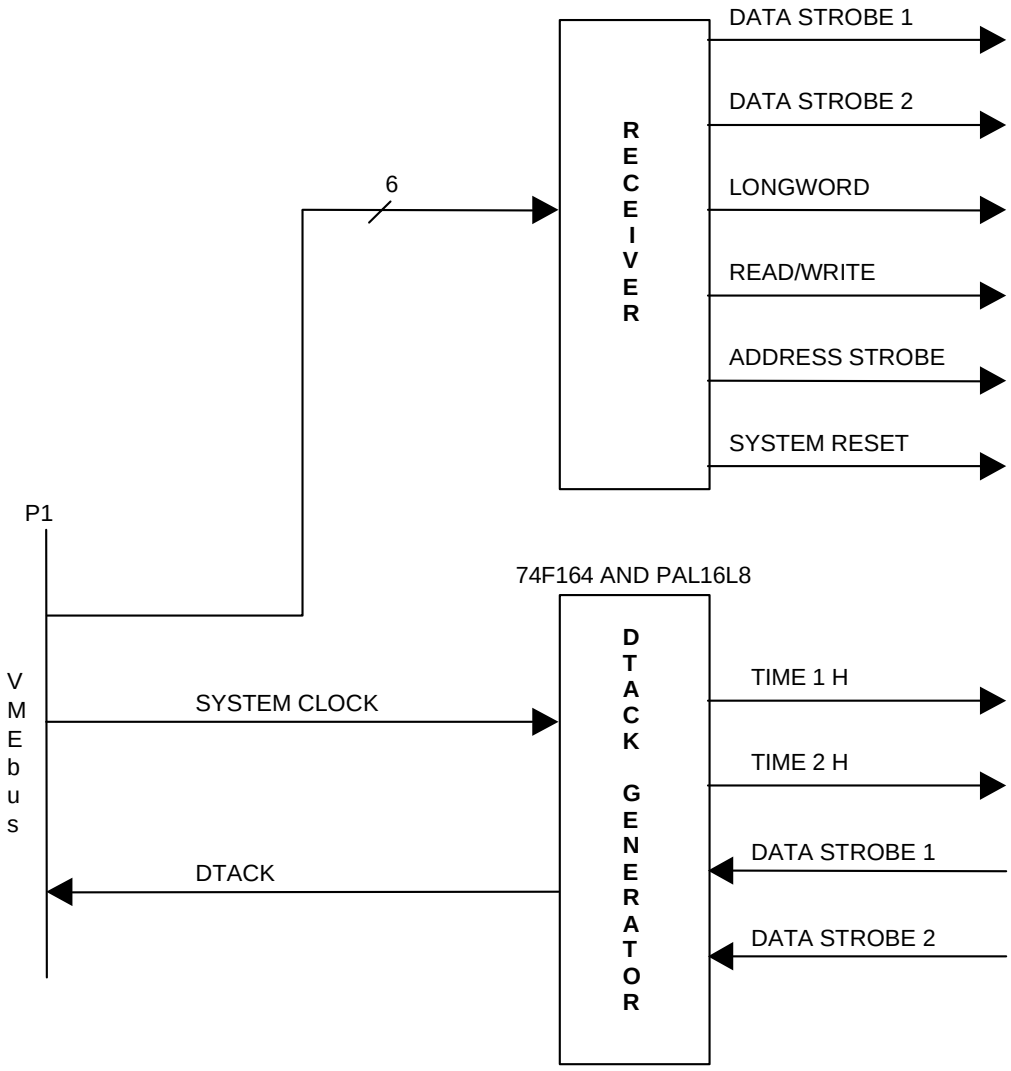


Figure 4-4: Address Selection Block Diagram

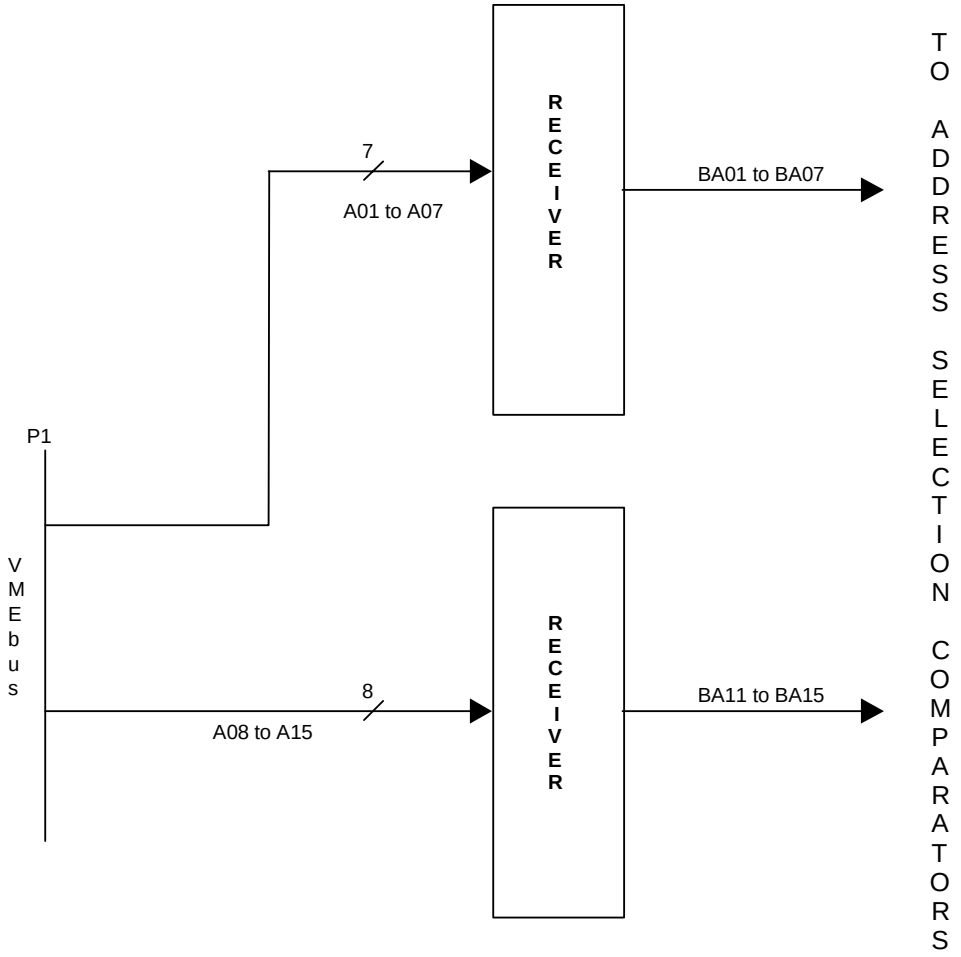


Figure 4-5: Data Transfer Block Diagram

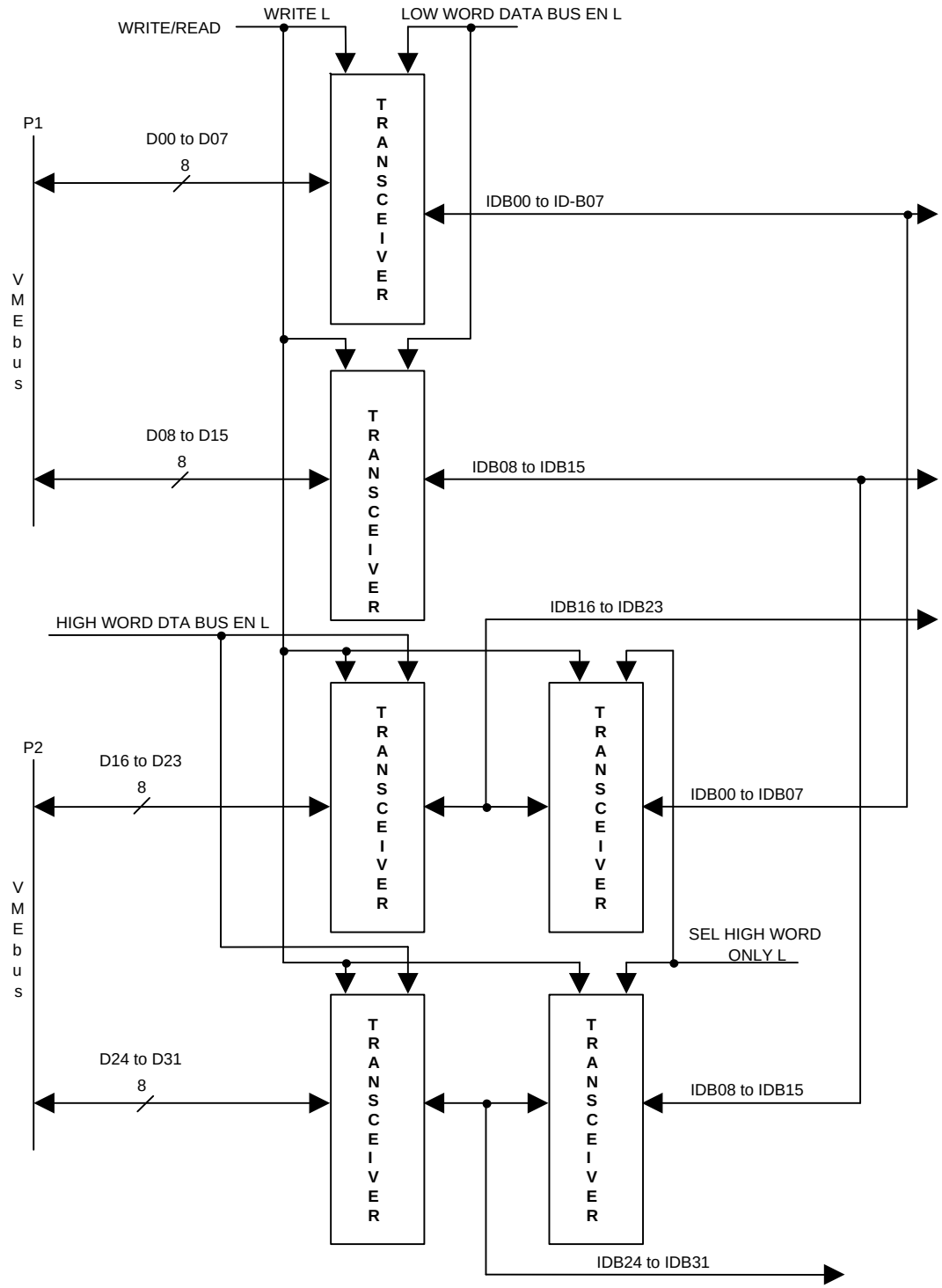
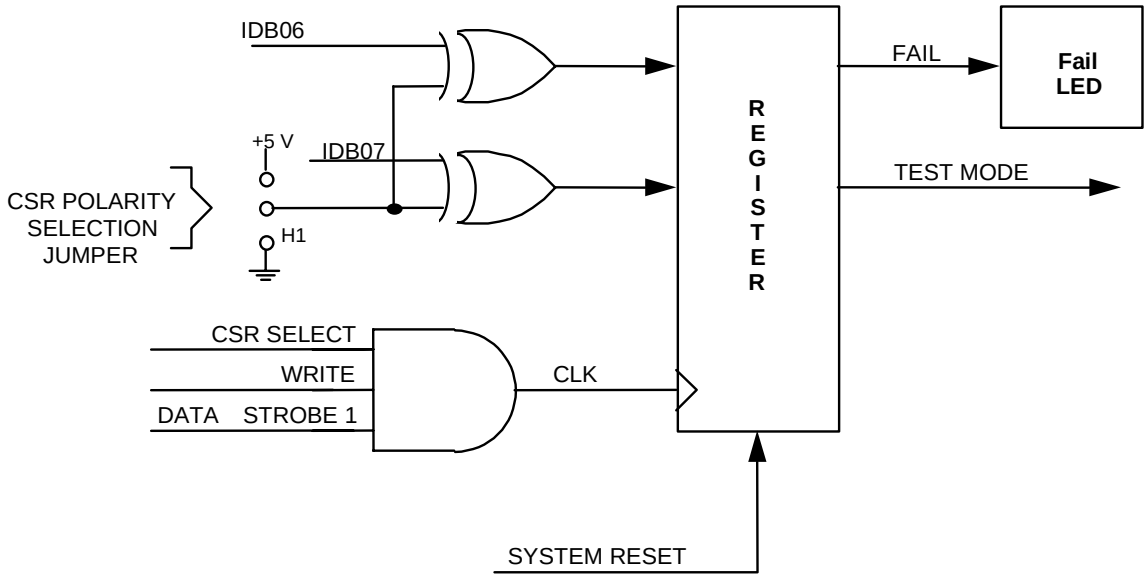


Figure 4-6: CSR Control Logic Block Diagram



# *Octal Registers and Output Drivers*

A block diagram of the eight 8-bit I/O registers is shown in Figure 4-7 on page 4-16 and Figure 4-8 on page 4-17. The Output Data Registers were selected as the primary building block of this design, because they have a unique feature that allows "read-back" of their input data, which is used by the Built-in-Test functions. In Test Mode, the Data Register outputs are tri-stated and the data read-back path is internal to the device. During normal operation, the data read-back path includes the output pins on the Output Data Register. Thus, during Test Mode all of the board's circuitry is tested, except for the output drivers.

Due to the large output currents possible, each driver pair has a separate pin for their source voltage and ground. This voltage is independent of the TTL control voltage driving the output devices. Its maximum value is determined by the output devices (UDN-2935ZH), which is 35 V. A detailed description of the output drivers is given in the product specification, Document Number GFK-2110.

**Caution**

**The user should use the cable ground lines for the external power supply returns. This is required to prevent excessive current from flowing into the VMEbus backplane. Also, the user should remove power before the cables are connected or disconnected (from the board). This will prevent excessive currents from damaging the P3/P4 connector pins.**

Figure 4-7: I/O Registers Block Diagram

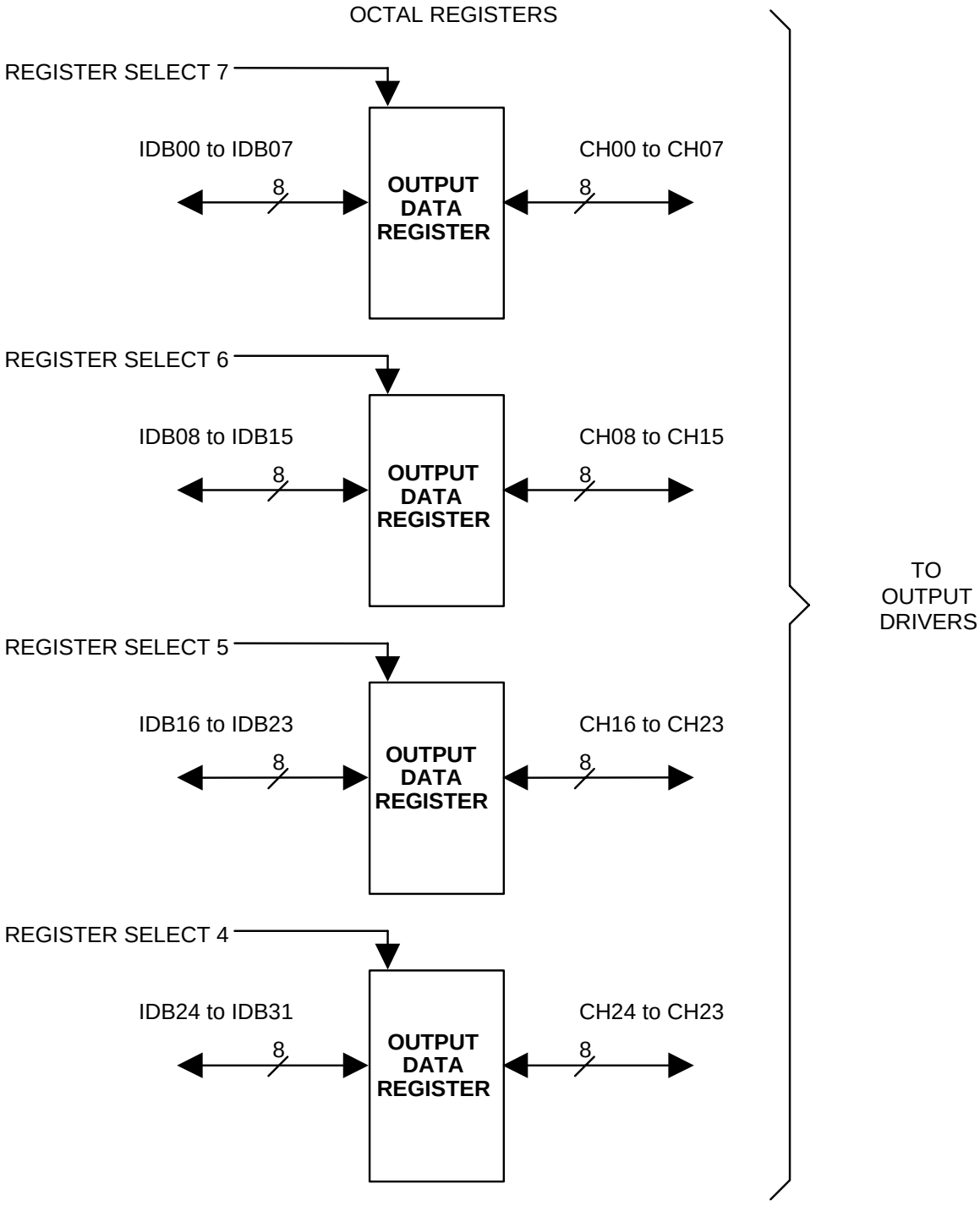
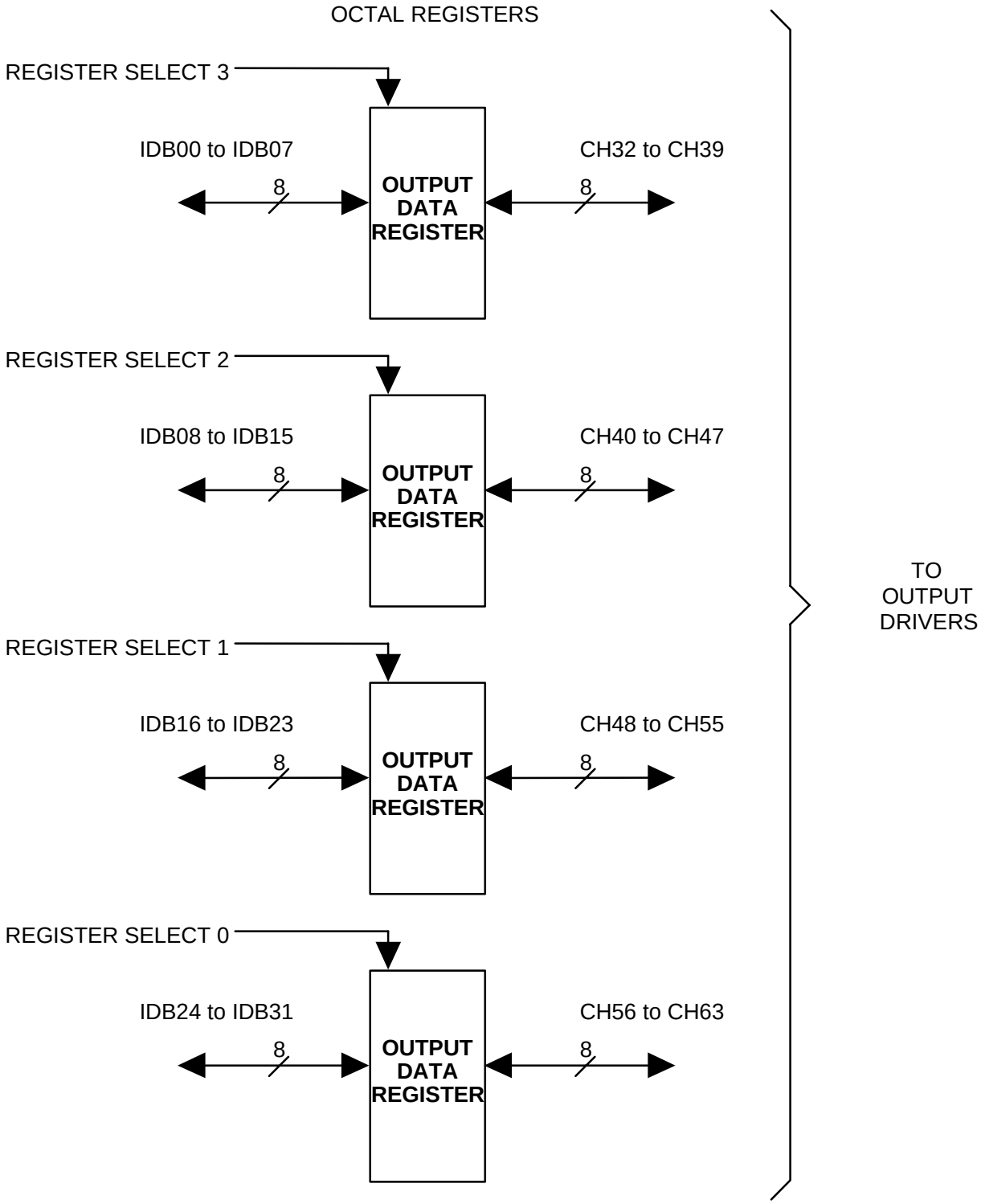


Figure 4-8: I/O Registers Block Diagram Bank B



# Chapter 5 Maintenance

This chapter provides information relative to the care and maintenance of the Digital Output Board product.

If the product malfunctions, verify the following:

- Software
- System configuration
- Electrical connections
- Jumper or configuration settings
- Boards fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the VMEbus card cage
- Quality of cables and I/O connections

User level repairs are not recommended. Contact your authorized GE Fanuc distributor for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**