GE Fanuc Automation

Programmable Control Products

IC697VDD100/IC697VDD125
64-Channel Isolated Digital Input Board
with Multifunctional Intelligent Controller

User's Manual

GFK-2062D 514-000440-000 E October 2005

Warnings, Cautions, and Notes as Used in this Publication

Warning

Warning notices are used in this publication to emphasize that hazardous voltages, currents, temperatures, or other conditions that could cause personal injury exist in this equipment or may be associated with its use.

In situations where inattention could cause either personal injury or damage to equipment, a Warning notice is used.

Caution

Caution notices are used where equipment might be damaged if care is not taken.

Note

Notes merely call attention to information that is especially significant to understanding and operating the equipment.

UL Information (applies to IC697VDD100 only)

1. EQUIPMENT LABELED WITH REFERENCE TO CLASS I, Div. 2, GROUPS A, B, C& D HAZARDOUS LOCATIONS IS SUITABLE FOR USE IN CLASS I, ZONE 2, GROUPS A, B, C, D OR NON-HAZARDOUS LOCATIONS ONLY.

2. EQUIPMENT LABELED WITH REFERENCE TO CLASS I, ZONE 2, GROUPS A, B, C & D HAZARDOUS LOCATIONS IS SUITABLE FOR USE IN CLASS I, ZONE 2, GROUPS A, B, C, D OR NON-HAZARDOUS LOCATIONS ONLY.

3. WARNING – EXPLOSION HAZARD – SUBSTITUTION OF COMPONENTS MAY IMPAIR SUITABILITY FOR CLASS I, DIVISION 2.

4. WARNING – EXPLOSION HAZARD – DO NOT DISCONNECT EQUIPMENT UNLESS POWER HAS BEEN SWITCHED OFF OR THE AREA IS KNOWN TO BE NON-HAZARDOUS.

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Chapter 1 Introduction, Description, and Specifications

This manual describes the installation and operation of the IC697VDD100/IC697VDD125 64-Channel Isolated Digital Input Board with Multifunctional Intelligent Controller.

Reference Material

For a detailed explanation of the VMEbus and its characteristics, “The VMEbus Specification” is available from:

VITA
VMEbus International Trade Association
7825 East Gelding Dr., No. 104
Scottsdale, AZ 85260
(480) 951-8866
FAX: (480) 951-0720
Internet: www.vita.com

General Overview

The Digital Input Board is a 64-channel optically isolated digital input board that can detect Changes of State (COS) on any of the 64 inputs. This COS data can be used in Sequence of Events (SOE) acquisition. The board provides pulse accumulation data, time tag data, and programmable debounce for each input. A variety of interrupt options are available. See Figure 1-1 on page 1-4 for more information.

The Digital Input Board features are outlined below.

- 64 optically isolated inputs
- Multiple-functions available per channel:
  - COS detection
  - SOE reporting
  - Pulse accumulation reporting
  - Time tag reporting
  - Programmable debounce times
- Available in 24VDC and 18VAC (IC697VDD100) or 125VDC and 110VAC (IC697VDD125) options
- Voltage sensing
- 1000 VDC or 700 VRMS channel-to-channel and channel-to-VMEbus isolation (1 minute)
- Pulse accumulation for up to 65,535 pulses per channel
- SOE monitoring on a channel-by-channel basis
- Debounce time software controlled on a channel-by-channel basis
- COS monitoring software controlled on a channel-by-channel basis
- A24/A16 addressing capability
- Supervisory bus access, nonprivileged bus access, or both
- Release-On-Acknowledge (ROAK) interrupts on all VMEbus levels

Functional Description

The Digital Input Board provides COS detection on all of its 64 inputs. Each input may be software controlled to detect rising edges, falling edges, or both rising and falling edges, or it may be software controlled to ignore all changes for a given channel. In addition to COS detection, a variety of reporting and interrupt capabilities are available.

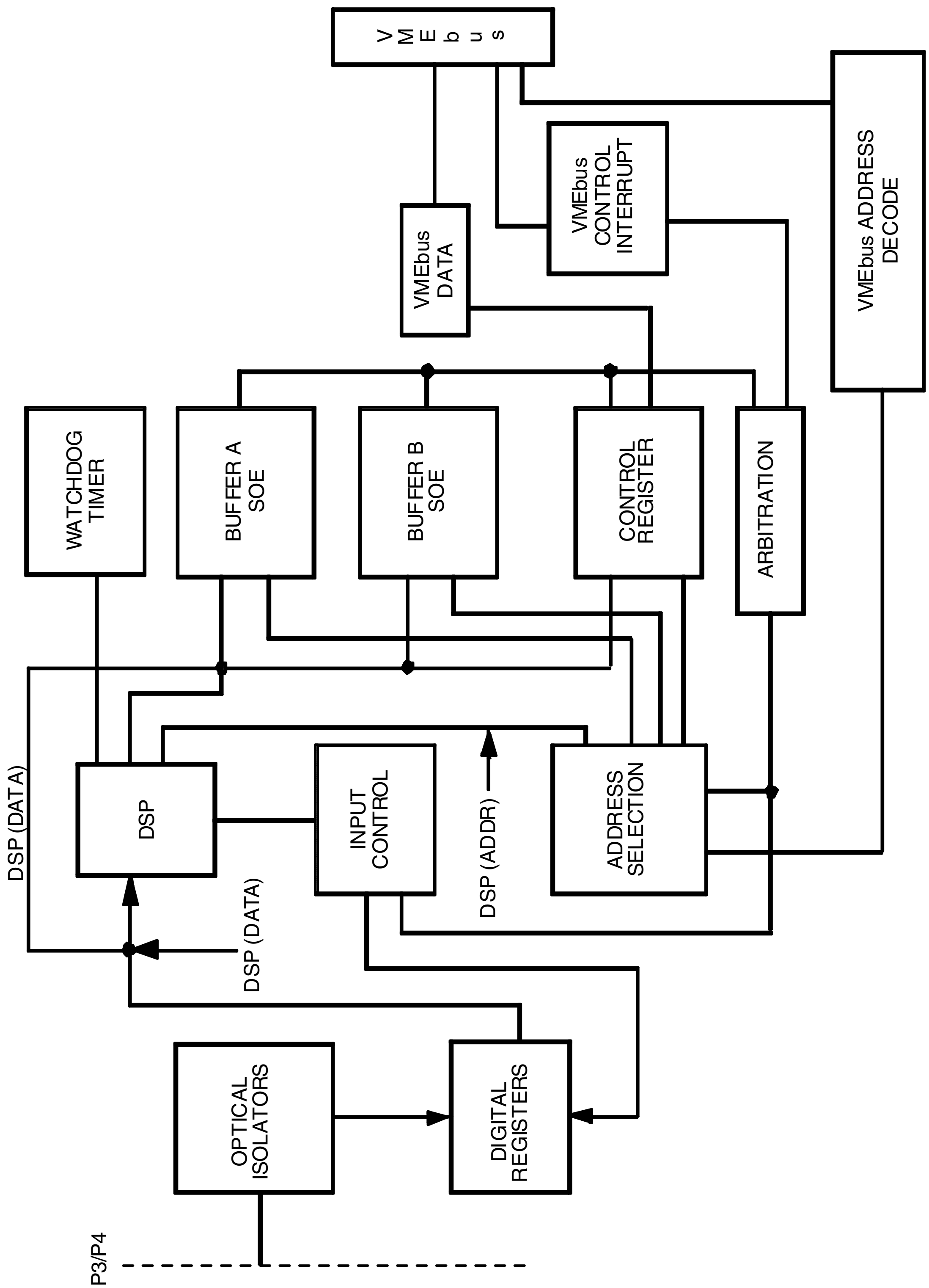
Each COS event may be stored in an SOE buffer where it is time tagged with a relative timer value of up to 65,535 ms. The timer may be reset from the VMEbus when desired. Each COS event is counted in Pulse Accumulation Count registers, which record the number of events per channel.

VMEbus interrupts may be issued on any level (software selectable), and a single byte vector is placed on the bus during the acknowledge cycle. The interrupt is cleared during the acknowledge (ROAK). Addressing is jumper selected and supports both A24 and A16 address space.

Address modifiers are jumper-selected and are decoded to support nonprivileged, supervisory, or both nonprivileged and supervisory access. A self-test is run automatically after a system reset, setting the Self-Test Complete bit in the Control and Status Register (CSR) to one when completed. The board is initialized with the following default conditions:

- Fail LED is ON.
- All interrupts are disabled.
- All flags are cleared.
- Test mode is enabled.
- Interrupt Vector Register (IVR) is cleared.
- COS registers are cleared.
- Pulse Accumulation Interrupt (PAI) registers are cleared.
- Input Debounce/Select Registers (DSRs) are cleared.
- Input Pulse Accumulation Count (PAC) registers are cleared.
- Time tag clock is set to zero (0) and stopped.
- SOEs maximum count is cleared.
- SOEs count is cleared.
- SOEs buffers contain test data, if self-test fails. If self-test passes, then the SOE buffers are cleared.
- Self-Test Complete bit is set in the CSR.

Figure 1-1: Digital Input Board Functional Block Diagram



Safety Summary

Warning

The following general safety precautions must be observed during all phases of this operation, service, and repair of this product. Failure to comply with these precautions or with specific warnings elsewhere in this manual violates safety standards of design, manufacture, and intended use of this product. GE Fanuc assumes no liability for the customer's failure to comply with these requirements.

Ground the System

To minimize shock hazard, the chassis and system cabinet must be connected to an electrical ground. A three-conductor AC power cable should be used. The power cable must either be plugged into an approved three-contact electrical outlet or used with a three-contact to two-contact adapter with the grounding wire (green) firmly connected to an electrical ground (safety ground) at the power outlet.

Do Not Operate in an Explosive Atmosphere

Do not operate the system in the presence of flammable gases or fumes. Operation of any electrical system in such an environment constitutes a definite safety hazard.

Keep Away from Live Circuits

Operating personnel must not remove product covers. Component replacement and internal adjustments must be made by qualified maintenance personnel. Do not replace components with power cable connected. Under certain conditions, dangerous voltages may exist even with the power cable removed. To avoid injuries, always disconnect power and discharge circuits before touching them.

Do Not Service or Adjust Alone

Do not attempt internal service or adjustment unless another person, capable of rendering first aid and resuscitation, is present.

Do Not Substitute Parts or Modify System

Because of the danger of introducing additional hazards, do not install substitute parts or perform any unauthorized modification to the product. Return the product to GE Fanuc for service and repair to ensure that safety features are maintained.

Chapter 2 Configuration and Installation

This chapter gives configuration and installation instructions for the Digital Input Board.

This chapter is divided into the following sections:

- Physical Installation
- Operational Configuration
- Field Input Configurations

Caution

Some of the components assembled on GE Fanuc's products may be sensitive to electrostatic discharge and damage may occur on boards that are subjected to a high energy electrostatic field. Unused boards should be stored in the same protective boxed in which they were shipped. When the boards is to be placed on a bench for configuring, etc., it is suggested that conductive material be inserted under the board to provide a conductive shunt.

Upon receipt, any precautions found in the shipping container should be observed. All items should be carefully unpacked and thoroughly inspected for damage that might have occurred during shipment. The board(s) should be checked for broken components, damaged circuit board(s), heat damage, and other visible contamination. All claims arising from shipping damage should be filed with the carrier and a complete report sent to GE Fanuc together with a request for advice concerning the disposition of the damaged item(s).

Physical Installation

Caution

Do not install or remove the boards while power is applied.

De-energize the equipment and insert the board into an appropriate slot of the chassis. While ensuring that the board is properly aligned and oriented in the supporting card guides, slide the board smoothly forward against the mating connector until firmly seated.

Operational Configuration

VMEbus access modes, address modes, and input configurations are controlled by field replaceable jumpers. This section describes the use of these jumpers and their effects on board performance. Locations and functions of all Digital Input Board jumpers are shown in Figure 2-1 on page 2-4 and Table 2-1 below.

Factory-Installed Jumpers

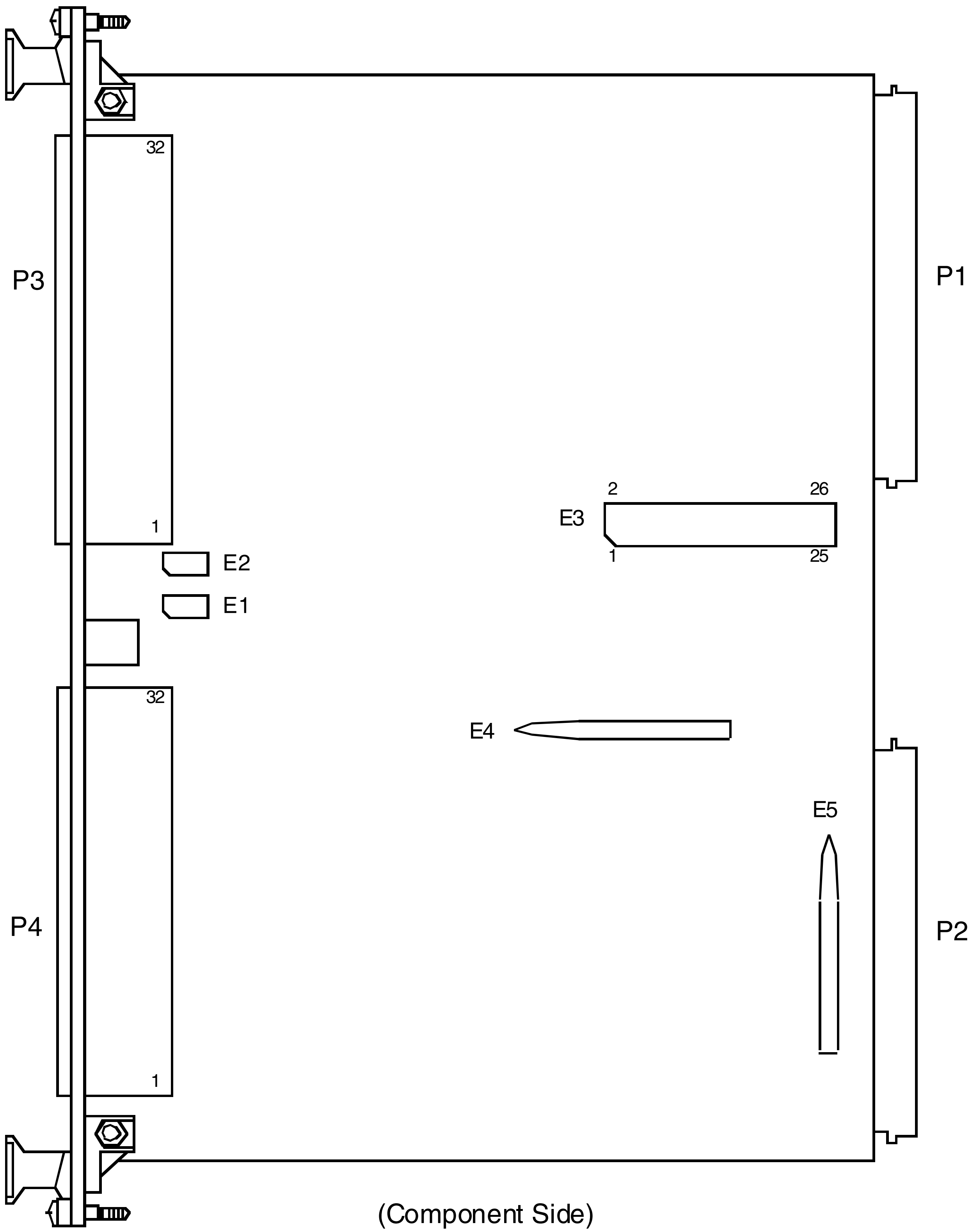
Each Digital Input Board is configured at the factory with the specific jumper arrangement shown in Table 2-1 below. The factory configuration ensures that all essential jumpers are installed and establishes the following functional baseline for the Digital Input Board:

- Board Identification is located at $000000 in the Standard I/O Space, with either Supervisory or Nonprivileged access.
- Wetting voltage application at P3 is disabled.
- Reference ground to P3 is disabled.
- Shorting plug of all external wetting voltages is disabled.

Table 2-1: Programmable Jumper Functions

Jumper ID	Function (Installed)	Factory Configuration
E3-1,2	Standard	Installed
E3-3,4	Supervisory or Nonprivileged	Installed
E3-5,6	Nonprivileged	Omitted
E3-7,8	Address Bit A14 = 0	Installed
E3-9,10	Address Bit A15 = 0	Installed
E3-11,12	Address Bit A16 = 0	Installed
E3-13,14	Address Bit A17 = 0	Installed
E3-15,16	Address Bit A18 = 0	Installed
E3-17,18	Address Bit A19 = 0	Installed
E3-19,20	Address Bit A20 = 0	Installed
E3-21,22	Address Bit A21 = 0	Installed
E3-23,24	Address Bit A22 = 0	Installed
E3-25,26	Address Bit A23 = 0	Installed
E1-1,2	CH32 Wetting Input at P3	Omitted
E2-1,2	Reference Ground at P3	Omitted
E4	Jumper Carrier	Installed
E5	Wetting Voltages tied together	Omitted

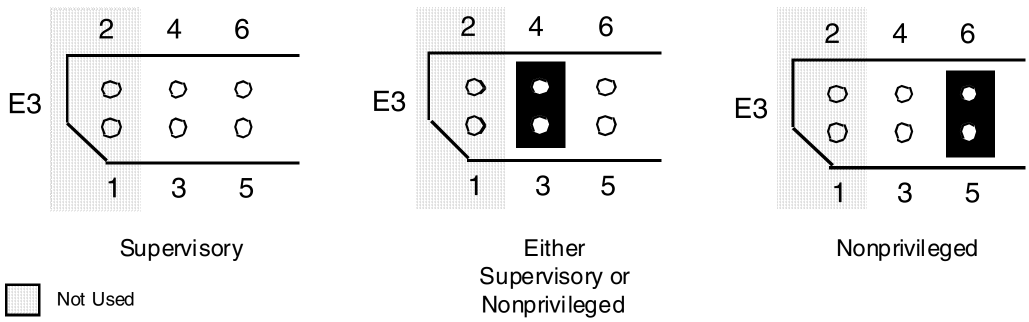
Figure 2-1: Configuration Jumpers and System Connectors



Access Modes

Supervisory or nonprivileged access is selected by pins 3 through 6 of jumper E3. Figure 2-2 below shows the jumper locations and access modes.

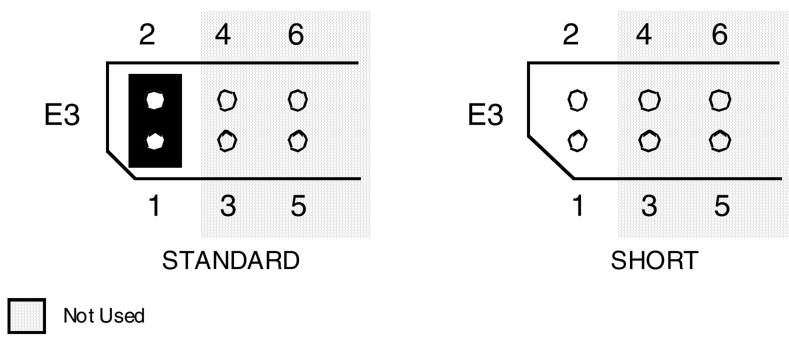
Figure 2-2: Supervisory and Nonprivileged Access Modes and Jumper Locations



Address Modes

Short I/O or Standard Addressing is selected by pins 1 and 2 of jumper E3. Figure 2-3 below shows the jumper locations and address modes.

Figure 2-3: Short I/O and Standard Addressing Modes and Jumper Locations

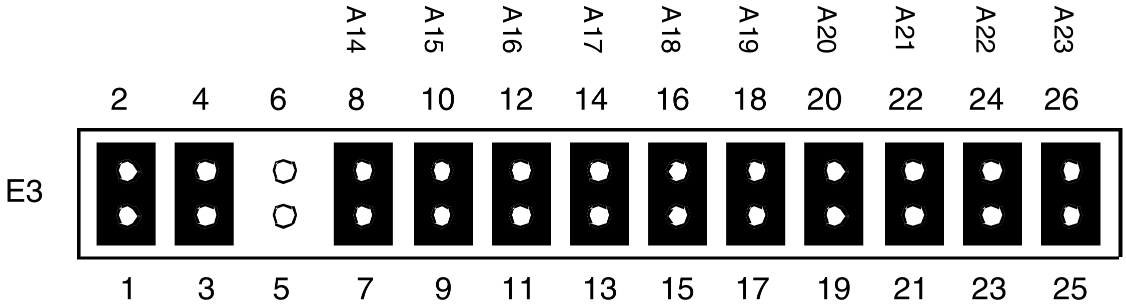


Board Address

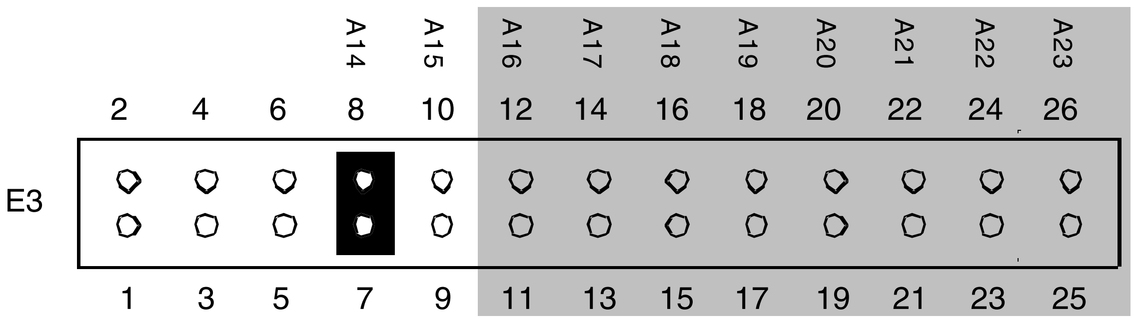
The board address is configured by pins 7 through 26 of jumper E3. The board supports A24/A16 addressing. The jumpers corresponding to the address bits are shown in Figure 2-4 on page 2-6. This figure also shows the factory configuration of E3 and example configurations.

The board address is programmed by installing shorting plugs at all zero (0) or LOW address bit positions in jumper field E3 and by omitting the shorting plugs at the one (1) or HIGH positions (ON = 0; OFF = 1).

Figure 2-4: Board Configuration Jumpers

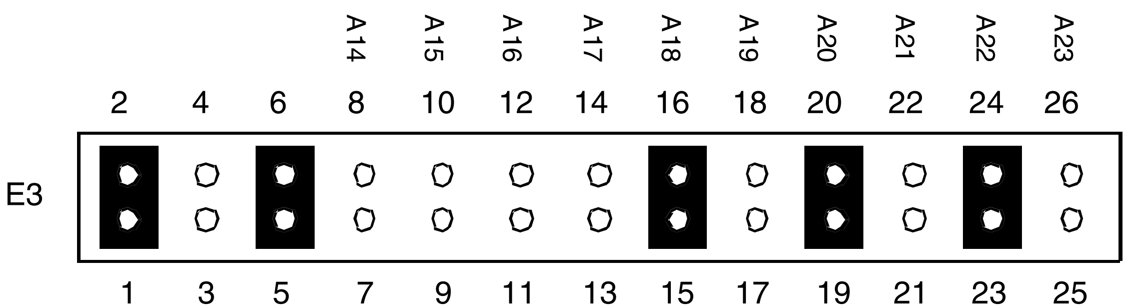


Factory Configuration
Standard Addressing, Supervisory or
Nonprivileged Access, $ 000000



Example Configuration
Short I/O Addressing, Supervisory Access,
$8000

Not Used



Example Configuration
Standard Addressing, Nonprivileged Access,
$ABC0 00

Field Input Configurations

The Digital Input Board provides factory configuration of voltage sensing input configurations. The four user-defined jumper fields for field inputs are described in the following sections.

Voltage Sensing

The user input connection circuit for voltage sensing is shown in Figure 2-5 below. Jumpers E1 and E4 are installed for this configuration. Jumpers E2 and E5 are omitted (see Table 2-2 below). This disables the wetting voltage input at P3 and allows channel 32 to be used as an input channel.

Figure 2-5: User Input Connection Circuit (Voltage Sensing)

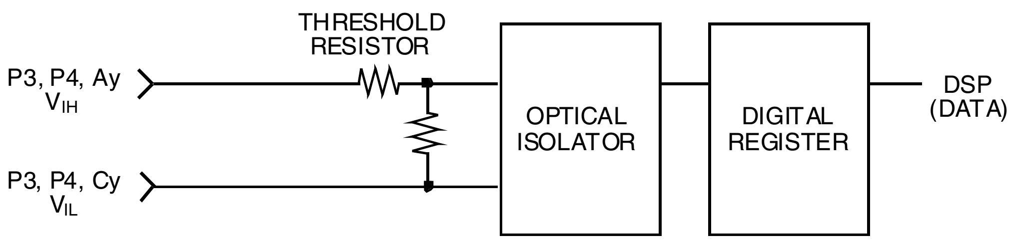


Table 2-2: Digital Input Board AB0 Jumper Placement for Voltage Sensing

Jumper Field	Function	Configuration
E1	Channel 32 enabled	Installed
E2	Reference Ground (Not at P3)	Omitted
E4	Carrier (No function)	Installed
E5	Wetting Voltages (Not tied together)	Omitted

System Connections

Table 2-3 below lists P2 connector pinout, Table 2-4 on page 2-9 lists P3 connector pinout, and the Table 2-5 on page 2-10 lists P4 connector pinout. The locations of the system interface connectors are shown in the Figure 2-1 on page 2-4. All inputs are available using two 64-pin front panel connectors.

Figure 2-6: P2 Connector

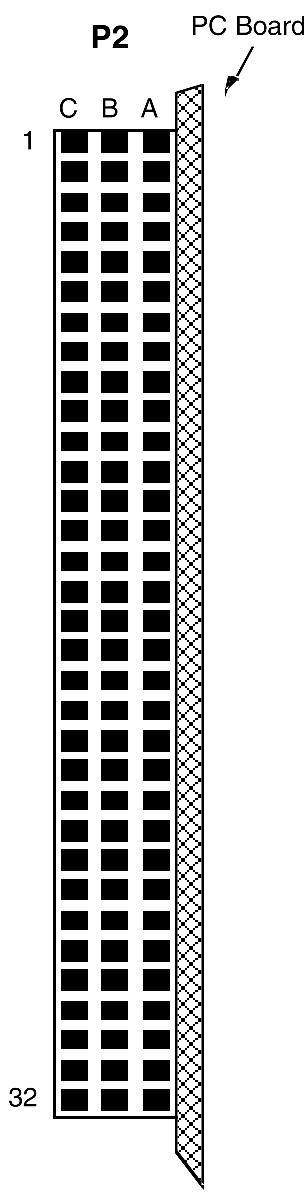


Table 2-3: P2 Connector Pinout

Pin	Row C	Row B	Row A	Pin	Row C	Row B	Row A
01	B0	+5V	DGND	17	DGND	N/C	N/C
02	B1	DGND	DGND	18	DGND	N/C	N/C
03	B2	N/C	DGND	19	V_{EXT}56	N/C	N/C
04	B3	N/C	DGND	20	DGND	N/C	N/C
05	B4	N/C	DGND	21	DGND	N/C	N/C
06	B5	N/C	DGND	22	V_{EXT}0	DGND	N/C
07	B6	N/C	DGND	23	DGND	N/C	N/C
08	B7	N/C	DGND	24	N/C	N/C	N/C
09	N/C	N/C	N/C	25	V_{EXT}8	N/C	N/C
10	V_{EXT}32	N/C	N/C	26	DGND	N/C	N/C
11	DGND	N/C	N/C	27	DGND	N/C	N/C
12	DGND	DGND	N/C	28	V_{EXT}16	N/C	DGND
13	V_{EXT}40	+5V	N/C	29	DGND	N/C	N/C
14	DGND	N/C	N/C	30	DGND	N/C	N/C
15	DGND	N/C	N/C	31	V_{EXT}24	DGND	N/C
16	V_{EXT}48	N/C	N/C	32	N/C	+5V	DGND

N/C = No Connection

Figure 2-7: P3 Connector

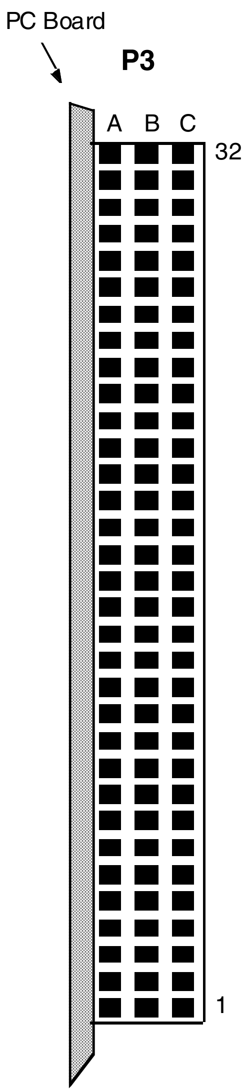


Table 2-4: P3 Connector Pinout

Pin	Row A	Row B	Row C	Pin	Row A	Row B	Row C
32	CH 63 HIGH	N/C	CH 63 LOW	16	CH 47 HIGH	N/C	CH 47 LOW
31	CH 62 HIGH	N/C	CH 62 LOW	15	CH 46 HIGH	N/C	CH 46 LOW
30	CH 61 HIGH	N/C	CH 61 LOW	14	CH 45 HIGH	N/C	CH 45 LOW
29	CH 60 HIGH	N/C	CH 60 LOW	13	CH 44 HIGH	N/C	CH 44 LOW
28	CH 59 HIGH	N/C	CH 59 LOW	12	CH 43 HIGH	N/C	CH 43 LOW
27	CH 58 HIGH	N/C	CH 58 LOW	11	CH 42 HIGH	N/C	CH 42 LOW
26	CH 57 HIGH	N/C	CH 57 LOW	10	CH 41 HIGH	N/C	CH 41 LOW
25	CH 56 HIGH	N/C	CH 56 LOW	09	CH 40 HIGH	N/C	CH 40 LOW
24	CH 55 HIGH	N/C	CH 55 LOW	08	CH 39 HIGH	N/C	CH 39 LOW
23	CH 54 HIGH	N/C	CH 54 LOW	07	CH 38 HIGH	N/C	CH 38 LOW
22	CH 53 HIGH	N/C	CH 53 LOW	06	CH 37 HIGH	N/C	CH 37 LOW
21	CH 52 HIGH	N/C	CH 52 LOW	05	CH 36 HIGH	N/C	CH 36 LOW
20	CH 51 HIGH	N/C	CH 51 LOW	04	CH 35 HIGH	N/C	CH 35 LOW
19	CH 50 HIGH	N/C	CH 50 LOW	03	CH 34 HIGH	N/C	CH 34 LOW
18	CH 49 HIGH	N/C	CH 49 LOW	02	CH 33 HIGH	N/C	CH 33 LOW
17	CH 48 HIGH	N/C	CH 48 LOW	01	CH 32 HIGH	N/C	CH 32 LOW *

* Channel 32 low can be used to obtain digital ground by the proper placement of on-board jumpers.

N/C = No Connection

Figure 2-8: P4 Connector

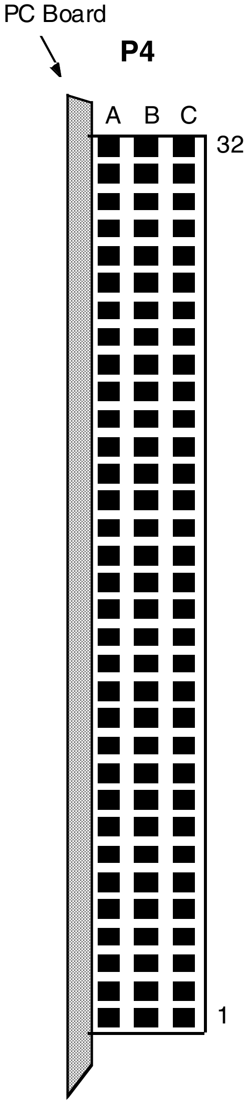


Table 2-5: P4 Connector Pinout

Pin	Row A	Row B	Row C	Pin	Row A	Row B	Row C
32	CH 31 HIGH	N/C	CH 31 LOW	16	CH 15 HIGH	N/C	CH 15 LOW
31	CH 30 HIGH	N/C	CH 30 LOW	15	CH 14 HIGH	N/C	CH 14 LOW
30	CH 29 HIGH	N/C	CH 29 LOW	14	CH 13 HIGH	N/C	CH 13 LOW
29	CH 28 HIGH	N/C	CH 28 LOW	13	CH 12 HIGH	N/C	CH 12 LOW
28	CH 27 HIGH	N/C	CH 27 LOW	12	CH 11 HIGH	N/C	CH 11 LOW
27	CH 26 HIGH	N/C	CH 26 LOW	11	CH 10 HIGH	N/C	CH 10 LOW
26	CH 25 HIGH	N/C	CH 25 LOW	10	CH 09 HIGH	N/C	CH 09 LOW
25	CH 24 HIGH	N/C	CH 24 LOW	09	CH 08 HIGH	N/C	CH 08 LOW
24	CH 23 HIGH	N/C	CH 23 LOW	08	CH 07 HIGH	N/C	CH 07 LOW
23	CH 22 HIGH	N/C	CH 22 LOW	07	CH 06 HIGH	N/C	CH 06 LOW
22	CH 21 HIGH	N/C	CH 21 LOW	06	CH 05 HIGH	N/C	CH 05 LOW
21	CH 20 HIGH	N/C	CH 20 LOW	05	CH 04 HIGH	N/C	CH 04 LOW
20	CH 19 HIGH	N/C	CH 19 LOW	04	CH 03 HIGH	N/C	CH 03 LOW
19	CH 18 HIGH	N/C	CH 18 LOW	03	CH 02 HIGH	N/C	CH 02 LOW
18	CH 17 HIGH	N/C	CH 17 LOW	02	CH 01 HIGH	N/C	CH 01 LOW
17	CH 16 HIGH	N/C	CH 16 LOW	01	CH 00 HIGH	N/C	CH 00 LOW

N/C = No Connection

Chapter 3 Programming

This chapter gives programming instructions for the Digital Input Board.

This chapter is divided into the following sections:

- Introduction
- Board ID Register (BID)
- Control and Status Register (CSR)
- Self-Test Results Register (STR)
- Interrupt Vector Register (IVR)
- Debounced Input Data Registers (IDR)
- COS Registers
- Pulse Accumulation Interrupt Registers (PAI)
- Debounce/Select Registers (DSR)
- Pulse Accumulation Count Registers (PAC)
- Time Tag Register
- Maximum SOE Count Register
- SOE Count Register
- SOE Index Register
- AC Input Register
- Revision Level Register
- Force LED Register
- SOE Request Register
- SOE Buffer Register

Introduction

The Digital Input Board can be programmed for a variety of features. After initial power up, system reset, or Watchdog Timer reset, the following conditions are initialized:

- Fail LED is ON.
- All interrupts are disabled.
- All flags are cleared.
- Test mode enabled.
- IVR register is cleared.
- COS registers are cleared.
- PAI registers are cleared.
- DSR registers are cleared.
- PAC registers are cleared.
- Time tag clock set to zero (0) and stopped.
- SOE maximum count is cleared.
- SOE count is cleared.
- SOE buffers contain test data, if self-test fails. Otherwise, the buffers are cleared.
- Self-Test Complete bit is set in the CSR.

If the initial conditions meet default requirements, then the user writes to the CSR to disable test mode and turn off the Fail LED. The user may then begin reading the input data registers which are updated with field data every millisecond. Table 3-1 on page 3-3 is the address map for the Digital Input Board. All addresses shown are relative to the board’s base address.

Note

To be consistent with conventional nomenclature, hexadecimal numbers in this document are designated with a “$” prefix unless otherwise indicated. Decimal numbers are presented without a prefix.

Table 3-1: Digital Input Board Memory Map

Relative Address	Description	Desig	Read/Write
$000	Board ID Register	BID	Read
$002	Control and Status Register	CSR	Read/Write
$004	Self-Test Results Register	STR	Read/Write
$006	Interrupt Vector Register	IVR	Read/Write
$008	Debounce Input Data for Channels 63-48	IDR 0	Read/Write
$00A	Debounce Input Data for Channels 47-32	IDR 1	Read/Write
$00C	Debounce Input Data for Channels 31-16	IDR 2	Read/Write
$00E	Debounce Input Data for Channels 15-00	IDR 3	Read/Write
$010	Change of State for Channels 63-48	COS 0	Read/Write
$012	Change of State for Channels 47-32	COS 1	Read/Write
$014	Change of State for Channels 31-16	COS 2	Read/Write
$016	Change of State for Channels 15-00	COS 3	Read/Write
$018	Pulse Accumulation Interrupt Chan 63-48	PAI 0	Read/Write
$01A	Pulse Accumulation Interrupt Chan 47-32	PAI 1	Read/Write
$01C	Pulse Accumulation Interrupt Chan 31-16	PAI 2	Read/Write
$01E	Pulse Accumulation Interrupt Chan 15-00	PAI 3	Read/Write
$020 - $09E	Debounce/Select Register (0-63)	DSR	Read/Write
$0A0 - $11E	Pulse Accumulation Count Register (0-63)	PAC	Read/Write
$120	Time Tag Register		Read/Write
$122	Maximum SOE Count Register		Read/Write
$124	SOE Count Register		Read/Write
$126	SOE Index Register		Read/Write
$128	Reserved (Note 1)		Read/Write
$12A	AC Input Register (default = 5)		Read/Write
$12C	Reserved (Note 1)		Read
$12E	Revision Level Register		Read
$130 - $7FE	Reserved (Note 1)		
$800	Force LED Register		Write
$802	SOE Request Register		Write
$804 - $9FE	Reserved (Note 1)		
$1000 - $3FFE	SOE Buffer Register		Read/Write

Must remain data = 0

Board ID Register (BID)

The BID register is a 16-bit read-only register. Its data is fixed at $3800. Table 3-2 below shows the bit map for this register.

Table 3-2: Board ID Register Bit Map

Relative Address $00 Board ID (read only)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	1	1	1	0	0	0
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
0	0	0	0	0	0	0	0

Control and Status Register (CSR)

The CSR is a 16-bit register that is used to control the operating parameters of the Digital Input Board. Table 3-3 below shows the bit map for this register.

Table 3-3: Control and Status Register Bit Map

Relative Address $002 CSR (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Fail LED	Test Mode	COS Reset	COS INT DIS	SOE WD INT EN	SOE CNT INT EN	PAC INT EN	TAG INT EN

Bit 07	Bit 06	Bit 05	Bit 04	Bit 03	Bit 02	Bit 01	Bit 00
SOE WD FL	SOE CNT FL	PAC FL	TAG FL	BUFF END FL	Reserved	Reserved	Self-Test Complete

Bit 15: **Fail LED** – Controls the Fail LED. Writing a zero (0) to this bit turns the Fail LED ON; writing a one (1) turns it OFF. The default condition is zero (0).

Bit 14: **Test Mode** – Controls the Test Mode. Writing a zero (0) to this bit initiates Test Mode. The default condition is zero (0). Test mode is enabled at power up, and the results are stored in the Self-Test Results register. To initiate test mode, the bit must be disabled by writing the bit to one (1) and then enabled by writing the bit to zero (0).

Bit 13: **COS Reset –** Clears the COS registers. Writing a one (1) to this bit clears all bits in the COS registers. After the COS registers are cleared, this bit is set to zero (0) by the microcontroller. After power up or reset, this bit is zero (0).

Bit 12: **COS INT DIS** – Controls the COS interrupts. Writing a one (1) to this bit disables the COS interrupts but allows COS data to be stored in the SOE buffer. The default condition is zero (0), allowing interrupts for any input meeting the requirements of its DSR.

Bit 11: **SOE WD INT EN** – Controls the SOE First Word interrupt. Writing a one (1) to this bit causes the board to interrupt the host whenever the first COS is received. The default condition is zero (0), which prevents an interrupt on this condition.

Bit 10: **SOE CNT INT EN** – Controls the SOE Buffer Count interrupt. Writing a one (1) to this bit causes the board to interrupt the host whenever the SOE count reaches the programmed value in the SOE Maximum Count register or when it reaches the physical end of memory. The default condition is zero (0), which prevents an interrupt on this condition.

Bit 09:	**PAC INT EN** – Controls the Pulse Accumulation Count Interrupt. Writing a one (1) to this bit causes the board to interrupt the host whenever any of the 64 PAC registers rolls over from a maximum count to zero (0) and sets the corresponding bit in the PAI registers. The default condition is zero (0), which prevents an interrupt on this condition.
Bit 08:	**TAG INT EN** – Controls the Time Tag Interrupt. Writing a one (1) to this bit causes the board to interrupt the host whenever the Time Tag Counter rolls over from maximum count to zero (0). The default condition is zero (0), which prohibits an interrupt on this condition.
Bit 07:	**SOE WD FL** – Set to one (1) whenever the first COS has been received and the SOE count equals one (1). The user must clear this bit by setting it to zero (0). This bit is active even if interrupts are disabled. The default condition is zero (0).
Bit 06:	**SOE CNT FL** – Set to one (1) whenever the SOE count has reached the preprogrammed value stored in the Maximum SOE Count register. The user must clear this bit by setting it to zero (0). This bit is active even if interrupts are disabled. The default condition is zero (0).
Bit 05:	**PAC FL –** Set to one (1) whenever any of the PAC registers ($0A0 through $11E) has rolled over. The user must clear this bit by setting it to zero (0). This bit is active even if interrupts are disabled. The corresponding bit (Channel ID) is set in the PAI register. The default condition is zero (0).
Bit 04:	**TAG FL** – Set to one (1) whenever a Time Tag overflow has occurred. The user must clear this bit by setting it to zero (0). This bit is active even if interrupts are disabled. The default condition is zero (0).
Bit 03:	**BUFF END FL –** Set to one (1) whenever the physical end of memory has been reached. The user must clear this bit by setting it to zero (0). The default condition is zero (0).
Bits 02 through 01:	**Reserved** – Reserved. The data must remain zero (0).
Bit 00:	**Self-Test Complete –** Set to one (1) whenever the self-test is complete. This bit is not cleared (set to zero (0)) when test mode is disabled.

Self-Test Results Register (STR)

The Digital Input Board performs Self-Test functions when one of the following conditions occur:

- VMEbus SYSRESET activated
- Watchdog Timer invokes a reset to the DSP
- Test Mode bit in CSR activated (The bit must be deactivated before it can be reactivated.)

The Self-Test of the Digital Input Board is performed by the DSP. Control memory and both SOE memory buffers are tested and the results stored in the Self-Test Status register located in control memory. The Self-Test mode is an integrity test of the DSP and the memory. The microcontroller sets the complete bit in the CSR but the user is responsible for clearing it and the STR register. Table 3-4 below shows the bit map for this register.

The STR contains a data pattern of $0CBA whenever the self-test is completed and passed.

Table 3-4: Self-Test Results Bit Map

Relative Address $004 STR (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
STR15	STR14	STR13	STR12	STR11	STR10	STR09	STR08

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
STR07	STR06	STR05	STR04	STR03	STR02	STR01	STR00

Bits 15 through 12 **STR [15:12]** – Always set to 0 (zero).

Bits 11 through 08: **STR [11:08]** – Set to $C whenever the Control Register Test has passed. This test is performed by the microcontroller by writing address equal data to the Control Register RAM. The data is then read and compared for accurate results. The control RAM is cleared after the results are posted.

Bits 07 through 04: **STR [07:04]** – Set to $B whenever Buffer B has been tested and passed. This test is performed by the microcontroller by writing an incremental (by 1) pattern from 0 through $17FF to the SOE buffer B RAM. The data is then read and compared for accurate results.

Bits 03 through 00: **STR [03:00]** – Set to $A whenever Buffer A has been tested and passed. This test is performed by the microcontroller by switching the buffer to A and writing a decremental pattern from $17FF through 0 to the SOE buffer A RAM. The data is then read and compared for accurate results.

Note

If self-test fails, then SOE buffer A and SOE buffer B test patterns are not cleared at the time the test complete bit of the CSR is set. If self-test passes, then the buffers are cleared before the test complete bit of the CSR is set.

Interrupt Vector Register (IVR)

The IVR is a 16-bit register used to enable any interrupts that may be set up in the CSR. Table 3-5 below shows the bit map of the IVR.

Table 3-5: Interrupt Control and Vector Register Bit Map

Relative Address $006 IVR (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Reserved	Reserved	Reserved	Reserved	Reserved	ILVL 2	ILVL 1	ILVL 0
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Vector bit 07	Vector bit 06	Vector bit 05	Vector bit 04	Vector bit 03	Vector bit 02	Vector bit 01	Vector bit 00

Bits 15 through 11: **Reserved –** These bits are reserved and must be set to zero (0).

Bits 10 through 08: **ILVL [2:0] –** Interrupt level bits. This field is used to select the VMEbus interrupt request level as shown in Table 3-6 below. The default is 000 (disabled).

Table 3-6: Interrupt Levels

VMEbus Interrupt Level	ILVL 2	ILVL 1	ILVL 0
Interrupts are disabled	0	0	0
IRQ1	0	0	1
IRQ2	0	1	0
IRQ3	0	1	1
IRQ4	1	0	0
IRQ5	1	0	1
IRQ6	1	1	0
IRQ7	1	1	1

Bits 07 through 00: **Vector [07:00] –** Interrupt vector bits. This field is used to select the VMEbus interrupt vector, which is presented during the interrupt acknowledge cycle.

Debounced Input Data Registers (IDR)

The Debounced Input Data registers are a set of four 16-bit registers which indicate the current state of the board inputs. Table 3-7 below lists the input channels and their associated register bit locations.

Table 3-7: Debounced Input Data Register Bit Map

Relative Address $008 Input Data Register 0 (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH 63	CH 62	CH 61	CH 60	CH 59	CH 58	CH 57	CH 56
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 55	CH 54	CH 53	CH 52	CH 51	CH 50	CH 49	CH 48

Relative Address $00A Input Data Register 1 (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH 47	CH 46	CH 45	CH 44	CH 43	CH 42	CH 41	CH 40
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 39	CH 38	CH 37	CH 36	CH 35	CH 34	CH 33	CH 32

Relative Address $00C Input Data Register 2 (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH 31	CH 30	CH 29	CH 28	CH 27	CH 26	CH 25	CH 24
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 23	CH 22	CH 21	CH 20	CH 19	CH 18	CH 17	CH 16

Relative Address $00E Input Data Register 3 (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 09	CH 08
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 07	CH 06	CH 05	CH 04	CH 03	CH 02	CH 01	CH 00

COS Registers

The COS registers are a set of four 16-bit registers. These registers are updated upon every change of state (if enabled). If the bit is a one (1), the input has had a change of state. These bits can be cleared by writing zero (0) to the registers or by writing a one (1) to bit 13 of the CSR. Bit 13 of the CSR is cleared when the COS registers are cleared. Table 3-8 below shows the bit map of the COS registers.

Table 3-8: COS Bit Map

Relative Address $010 COS Register 0 (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH 63	CH 62	CH 61	CH 60	CH 59	CH 58	CH 57	CH 56
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 55	CH 54	CH 53	CH 52	CH 51	CH 50	CH 49	CH 48

Relative Address $012 COS Register 1 (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH 47	CH 46	CH 45	CH 44	CH 43	CH 42	CH 41	CH 40
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 39	CH 38	CH 37	CH 36	CH 35	CH 34	CH 33	CH 32

Relative Address $014 COS Register 2 (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH 31	CH 30	CH 29	CH 28	CH 27	CH 26	CH 25	CH 24
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 23	CH 22	CH 21	CH 20	CH 19	CH 18	CH 17	CH 16

Relative Address $016 COS Register 3 (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 09	CH 08
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 07	CH 06	CH 05	CH 04	CH 03	CH 02	CH 01	CH 00

Pulse Accumulation Interrupt Registers (PAI)

The Pulse Accumulation Interrupt registers are a set of four 16-bit registers. These registers indicate that the pulse accumulation count for that channel has rolled over from a maximum count to zero (0). The user may clear these bits at any time. Table 3-9 below shows the bit map of the PAI registers.

Table 3-9: PAI Register Bit Map

Relative Address $018 PAI Register 0 (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH 63	CH 62	CH 61	CH 60	CH 59	CH 58	CH 57	CH 56

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 55	CH 54	CH 53	CH 52	CH 51	CH 50	CH 49	CH 48

Relative Address $01A PAI Register 1 (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH 47	CH 46	CH 45	CH 44	CH 43	CH 42	CH 41	CH 40

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 39	CH 38	CH 37	CH 36	CH 35	CH 34	CH 33	CH 32

Relative Address $01C PAI Register 2 (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH 31	CH 30	CH 29	CH 28	CH 27	CH 26	CH 25	CH 24

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 23	CH 22	CH 21	CH 20	CH 19	CH 18	CH 17	CH 16

Relative Address $01E PAI Register 3 (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CH 15	CH 14	CH 13	CH 12	CH 11	CH 10	CH 09	CH 08

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CH 07	CH 06	CH 05	CH 04	CH 03	CH 02	CH 01	CH 00

Debounce/Select Registers (DSR)

The Debounce Select registers are a set of 64, 16-bit registers. These registers control what conditions define a COS for that channel as well as the debounce time for that channel. If a COS is defined for a channel, the SOE Buffer is updated each time a COS is detected. Table 3-10 below shows the bit map for the Debounce/Select register for channel 0. All DSRs follow the same map.

Table 3-10: Debounce/Select Registers

Relative Address $20 DSR Register (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
COS 1	COS 0	AC EN	Reserved	Reserved	Reserved	DEB 09	DEB 08
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
DEB 07	DEB 06	DEB 05	DEB 04	DEB 03	DEB 02	DEB 01	DEB 00

Bits 15 through 14: **COS [01:00]** – COS Select bits (see Table 3-11 below).

Table 3-11: COS Select Bits

COS 1	COS 0	COS Definition/Detection
0	0	COS Definition/Detection Disabled
0	1	COS Definition/Detection on falling edge
1	0	COS Definition/Detection on rising edge
1	1	COS Definition/Detection on both edges*

Bit 13: **AC EN** – Controls COS algorithm. Writing a one (1) to this bit enables COS detection for AC input voltages. The default condition is zero (0). Revision Level Register on page 20 describes typical debounce select time when using AC Input.

Bits 12 through 10: **Reserved** – These bits are reserved and must be set to zero (0).

Bits 09 through 00: **DEB [09:00]** – Debounce Timer Select may be set from 1 MS through 1.024 seconds. See Table 3-12 on page 3-13 for a description of the bit weight.

Table 3-12: Debounce Timer Select

Bits 9 through 0	Debounce Rate
$000	1 ms
$001	2 ms
$002	3 ms
•	•
•	•
•	•
$3FD	1.022 s
$3FE	1.023 s
$3FF	1.024 s

Pulse Accumulation Count Registers (PAC)

The Pulse Accumulation Count registers are a set of 64, 16-bit registers. These registers are incremented each time a COS is detected on the corresponding input. In the event of a rollover, the corresponding bit is set in the PAI registers and a flag is set in the CSR. These registers may be preset to any value. Table 3-13 below shows the bit map for one of the Pulse Accumulation Count registers. All PAC registers follow the same map. This function is not implemented if COS 1 and COS 0 of the DSR are both zero (0) or both one (1).

Table 3-13: Pulse Accumulation Count Register Bit Map

Relative Address $0A0 PAC Register (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
PAC 15	PAC 14	PAC 13	PAC 12	PAC 11	PAC 10	PAC 09	PAC 08
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
PAC 07	PAC 06	PAC 05	PAC 04	PAC 03	PAC 02	PAC 01	PAC 00

Time Tag Register

The Time Tag register stores the current value of the 16-bit timer which is used for time tagging the COS data in the SOE buffer. The Time Tag counter is a free-running counter which can be preset during non-test mode. At maximum count, the board sets a flag in the CSR and issues an interrupt to the host if the Time Tag Rollover interrupt is enabled in the CSR. Table 3-14 below shows the bit map of the Time Tag register. The bit weight is 1 ms.

Table 3-14: Time Tag Register Bit Map

Relative Address $120 Time Tag Register (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Time Tag MSB							

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Time Tag LSB							

Maximum SOE Count Register

The Maximum SOE Count register is a 16-bit register. This register enables the user to program the maximum count of events before an SOE buffer count interrupt occurs. If the maximum count is reached, the board sets a flag in the CSR and interrupts the host if the SOE count interrupt is enabled in the CSR. See Table 3-15 below for bit definitions.

The Maximum SOE Count should be set for $C00 or less. $C00 represents the last SOE event that can be stored. Any further events overwrite the beginning of the buffer resulting in a loss of data.

Table 3-15: Maximum SOE Count Bit Map

Relative Address $122 Maximum SOE Count (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
MAX 15	MAX 14	MAX 13	MAX 12	MAX 11	MAX 10	MAX 09	MAX 08

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
MAX 07	MAX 06	MAX 05	MAX 04	MAX 03	MAX 02	MAX 01	MAX 00

SOE Count Register

The SOE Count register is a 16-bit register which indicates the present count of events in the SOE buffer currently being updated by the microcontroller. The register is initialized at system reset. When an SOE Request is received, the count is written to the SOE index register and then reset. Table 3-16 below shows the SOE Count register bit map.

Table 3-16: SOE Count Bit Map

Relative Address $124 SOE Count (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CNT 15	CNT 14	CNT 13	CNT 12	CNT 11	CNT 10	CNT 09	CNT 08

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CNT 07	CNT 06	CNT 05	CNT 04	CNT 03	CNT 02	CNT 01	CNT 00

SOE Index Register

The SOE Index represents the SOE count of the buffer available to the VMEbus. Table 3-17 below shows the bit map of the SOE Index register.

Table 3-17: SOE Index Bit Map

Relative Address $126 SOE Index (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
CNT 15	CNT 14	CNT 13	CNT 12	CNT 11	CNT 10	CNT 09	CNT 08
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
CNT 07	CNT 06	CNT 05	CNT 04	CNT 03	CNT 02	CNT 01	CNT 00

AC Input Register

To designate a particular channel as an AC input, write the default value $0005 to the AC Input register and set the AC EN control bit to one (1) in the associated DSR. Adjust the debounce time and COS parameters as described in Debounce/Select Registers (DSR) on page 3-12.

AC inputs are detected as pulse trains with assumed duty cycles of approximately 35 percent. Consequently, the delay time for a LOW-to-HIGH transition is determined by input sensitivity and may vary as much as 50 percent from the selected debounce time. Delay times for HIGH-to-LOW transitions, however, are not affected by input sensitivity and should agree closely with selected debounce times.

Debounce times for AC inputs should be selected to include at least five complete cycles of the AC input waveform. For example, debounce times for 50 Hz inputs (period equals 20 ms) should not be less than 100 ms.

Revision Level Register

The value in this register corresponds to the part description in the assembly drawing for the EPROM on the Digital Input Board.

Force LED Register

The Force LED is a write-only (data = don't care) register which forces the front panel LED on. If Force LED is activated, the CSR bit 15 is ignored, and the LED can only be turned off by a VMEbus system reset. See Table 3-18 below for the Force LED bit map.

Table 3-18: Force LED Bit Map

Relative Address $800 Force LED (write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
X	X	X	X	X	X	X	X

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
X	X	X	X	X	X	X	X

X = Don't Care

SOE Request Register

The SOE Request is a write-only (data = don't care) register. A write to this register allows the user access to the SOE data, copies the SOE count to the SOE Index register, and resets the SOE count. Table 3-19 below shows the bit map of the SOE Request register.

Table 3-19: SOE Request Bit Map

Relative Address $802 Buffer Access (write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
X	X	X	X	X	X	X	X
Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
X	X	X	X	X	X	X	X

X = Don't Care

SOE Buffer Registers

The SOE Buffer is a set of 6144, 16-bit registers capable of storing 3072 events. If the user issues a SOE Request, the board may continue to store up to 3072 more events while the user is processing the present buffer.

Caution

The DSP will auto wrap the buffer and begin writing over old data whenever the buffer reaches the physical end of the buffer. The SOE count rolls over from 3072 to zero (0) and continues counting. The host must process the data from the primary buffer before the DSP reaches the physical end of the data buffer or data can be lost. Interrupts are provided (SOE maximum count) to alert the host that data needs to be processed.

The event data stored in the SOE buffer consists of two words. Word 1 is a 16-bit time stamp as read from the Time Tag register when the COS occurred. The Channel ID is located in word 2 in the lower byte (bits 7 through 0). If the state changed from a zero (0) to a one (1), bit 8 of word 2 is set to a one (1). If the state changed from a one (1) to a zero (0), bit 8 of word 2 is set to a zero (0). Table 3-20 below is a bit map of one SOE buffer. All SOE buffers follow the same map.

Table 3-20: SOE Buffers Bit Map

Relative Address $1000 SOE Buffer Word 1 (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
Time Tag MSB							

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Time Tag LSB							

Relative Address $1002 SOE Buffer Word 2 (read/write)							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 09**	**Bit 08**
0	0	0	0	0	0	0	LVL

Bit 07	**Bit 06**	**Bit 05**	**Bit 04**	**Bit 03**	**Bit 02**	**Bit 01**	**Bit 00**
Channel ID							

Chapter 4 Theory of Operation

This chapter describes the internal organization of the Digital Input Board and reviews the general principles of operation. Major board functions are both summarized and individually described later in this chapter. Programming details in chapter 3 supplement this chapter, which is divided into the following sections:

- Internal Functional Organization
- Field Inputs
- Input Data Processing
- VMEbus Interface
- Bus Interrupter
- Watchdog Timer
- Self-Test
- Power Requirements

Internal Functional Organization

The Digital Input Board is a 64-channel optically isolated digital input board that provides the user with a continuous update of the state of the 64 inputs. The user may elect to interrupt the host upon selected COS events. COS data and time tag information is stored in memory (SOE monitoring) for later processing.

The SOE memory is allocated into two buffers which store the COS data with a sequential time tag for each event in the order that they occurred. The host can process the SOE buffer without losing any COS data from the inputs.

The Digital Input Board provides a Pulse Accumulation Count register for each channel. When enabled, these registers each store a count representing the number of times a COS has occurred on its associated input.

Inputs can be programmed individually for a debounce time from 1 ms to 1.023 seconds.

The board design can be logically divided into functional blocks which describe the following principal hardware functions:

- Field Inputs
- Input Data Processing by the Digital Signal Processor (DSP)
- EPROM
- VMEbus Interface
- Control Logic
- Bus Interrupter
- Watchdog Timer
- Self-Test
- Power Requirements

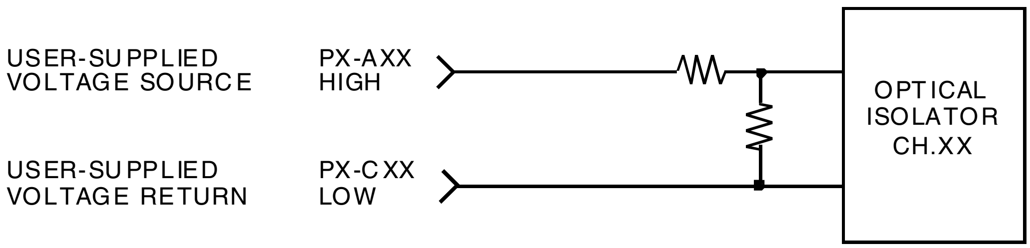
Field Inputs

The field inputs consist of 64 optically isolated inputs. The inputs are provided through connectors P3 and P4. Chapter 2 provides detailed information about both of these connectors.

Voltage Sensing

The Voltage Sensing option detects the presence or absence of a voltage at the inputs. Figure 4-1 below shows typical voltage sensing input circuitry.

Figure 4-1: Voltage Sensing Input Circuit



Input Data Processing

The Digital Input Board provides various programmable features. In default mode, the inputs are stored every millisecond and can be accessed by the user at any time. The programmable features are executed through an on-board Digital Signal Processor (DSP) chip and include:

- Debounce time for each input
- Pulse accumulation for each input
- COS definition/selection for each input
- Time tag clock
- SPE monitoring

Each feature is described in the following paragraphs.

Debounce Time

The Digital Input Board provides 64 registers which contain the desired debounce time for each input. The debounce time ranges from 1 ms (default) to 1.024 seconds. See chapter 3 for more information on selecting debounce times.

The debounce algorithm is implemented by the DSP microcontroller. Through the optical isolator, all 64 field inputs are clocked into registers during the DSP time interrupt service routine. The DSP processes this data using an algorithm which determines a true high or low state.

A different algorithm may be used by setting a bit in the Debounce/Select Register (see chapter 3). This algorithm accepts inputs from AC signal sources. The rising edge period is determined by the Debounce/Select time provided by the user. The falling edge period requires the DSP to detect a low at four times the debounce time in milliseconds. This ratio, the AC Ratio, is defined in chapter 3.

Pulse Accumulation

Each channel has an associated Pulse Accumulation Count (PAC) register. The count represents 0 to 65,535 pulses. A pulse is defined as either a state change from zero (0) to one (1) or a state change from one (1) to zero (0), but not both. If the PAC Interrupt Enabled bit is activated, the PAC register interrupts the host when it rolls over to zero (0).

COS Definition

Each channel can be programmed to detect rising edge (low to high) only, falling edge (high to low) only, both edges, or no detection (COS disabled). Interrupts can be issued when any input meets the programmable COS selection. A detailed description of this function is found in chapter 3.

Time Tag Clock

The Time Tag register is updated every millisecond. The user may reset or preset this data at any time. The Time Tag feature is provided by the DSP Timer Interrupt Logic and microcontroller. The microcontroller is interrupted every millisecond. During the interrupt service routine, the field inputs are stored and a frame flag is updated. A frame is the period in which all 64 inputs have been processed. Every frame, the DSP updates the Time Tag data. Each bit of the count in the Time Tag register represents 1 ms.

Sequence of Event

Depending on COS select settings, each COS can be time tagged in the SOE buffer. The SOE buffer collects the channel ID and the time in which the state changed. This buffer can contain 3072 events. When the host is accessing the SOE buffer, the Digital Input Board continues to monitor the inputs and stores events in a mirrored SOE buffer. The additional buffer also provides 3072 events of storage, allowing the user sufficient time to process the SOE data without losing event data. The SOE logic can provide an interrupt to the host at the end-of-buffer or at a count provided by the user.

The SOE buffer arbitration is controlled by software. To read the data in the SOE buffer, the host first writes to the SOE Request register. A write to this register interrupts the DSP code and switches the pointer in the DSP to the second SOE buffer. The VMEbus then has access to the first SOE buffer while the DSP continues its updates to a second SOE buffer. This method allows the DSP to always have access to one of the SOE buffers in order to prevent data loss.

Caution

The DSP will auto wrap the buffer and begin writing over old data whenever the buffer reaches the physical end of the buffer. The SOE count rolls over from 3072 to zero (0) and continues counting. The host must process the data from the primary buffer before the DSP reaches the physical end of the data buffer or data can be lost. Interrupts are provided (SOE maximum count) to alert the host that data needs to be processed.

The SOE count is valid for whichever SOE buffer the DSP is currently updating. Once the buffer is requested, the SOE count is written to the SOE index and then reset to zero (0).

EPROM

DSP firmware is stored in the EPROM and is loaded into the DSP during power up or after a reset to the DSP. The DSP can be reset by the VMEbus system reset or by the Watchdog Timer circuitry.

VMEbus Interface

The VMEbus interface consists of:

- Address decoding for the A24/A16 address space
- Address modifier decoding for supervisory/nonprivileged accesses
- D16/D8 data transfers
- ROAK interrupter circuitry
- Two SOE buffers
- Control logic memory

Control Logic

The Control Logic offset address begins at $000. The Board ID register contains an ID code which indicates the Digital Input Board is present. The Control and Status register provides control of the front panel LED, the Test Mode Disable, and various interrupt enables. It also provides various flags, including a Self-Test complete flag.

The Self-Test Results register provides pass/fail status of the Digital Input Board integrity tests. The Interrupt Vector register provides programmable level and vector data. Debounced input data is provided in four words, each bit representing a channel. Change of State registers are provided in four words, each bit representing a channel. Pulse Accumulation Interrupt registers are provided in four words, each bit representing a channel. Each channel has an associated Debounce/Select register and Pulse Accumulation Count register.

A Time Tag register is provided and is updated every millisecond. Three registers are provided to support SOE buffer function: the Maximum SOE Count, the SOE Count, and the SOE Index.

When used in conjunction with the Debounce/Select registers, the AC Input register provides debounce with AC input.

Bus Interrupter

A Bus Interrupter provides access to the VMEbus interrupt structure. An interrupt can be issued on any level (software selectable), and a single byte vector is placed on the bus when acknowledged. Any of the following conditions can initiate the interrupt:

- COS on any of the 64 channels
- Time Tag rollover
- Pulse Accumulation rollover on any of the 64 channels
- SOE, End-of-Buffer, First Word Received
- SOE buffer count equal to programmable maximum count provided by the user

Each of these interrupt conditions may be enabled or disabled by the host. A global disable occurs if the interrupt level is set to zero (0). There is one ROAK interrupt for the Digital Input Board board. Details of the interrupter capabilities are described in chapter 3.

Watchdog Timer

The Digital Input Board monitors the health of the DSP and resets it if necessary. The DSP must write to a specified address every millisecond or the Watchdog Timer will issue a reset to the DSP. A reset to the DSP results in reloading the EPROM data and reinitializing the default conditions. The Digital Input Board is off-line at this time. This circuitry also monitors the general integrity of the +5 V on the VMEbus and issues a reset to the DSP if it falls below +4.5 V.

Self-Test

The Digital Input Board performs Self-Test functions when one of the following conditions occur:

- VMEbus SYSRESET activated
- Watchdog Timer invokes a reset to the DSP
- Test Mode bit in CSR activated

The DSP performs the Self-Test of the Digital Input Board. Control memory and both SOE memory buffers are tested, and the results stored in the Self-Test Status register located in control memory. The Self-Test mode is an integrity test of the DSP and the memory. The field input connectors to the digital registers are not tested on-board. The VMEbus-to-Digital-Input-Board memory is not tested in Self-Test mode. System test software is responsible for determining these functions and for turning the front panel LED off when the system has determined that the Digital Input Board has passed.

Power Requirements

Power Requirements for the Digital Input Board are:

2.0A (typical) at 5V plus any power dissipated in pull-up resistors.

Chapter 5 Maintenance

Maintenance

This chapter provides information relative to the care and maintenance of the Digital Input Board product.

If the product malfunctions, verify the following:

- Software
- System configuration
- Electrical connections
- Jumper or configuration settings
- Boards are fully inserted into their proper connector location
- Connector pins are clean and free from contamination
- No components of adjacent boards are disturbed when inserting or removing the board from the chassis
- Quality of cables and I/O connections

User level repairs are not recommended. Contact your authorized GE Fanuc distributor for a Return Material Authorization (RMA) Number. **This RMA Number must be obtained prior to any return.**